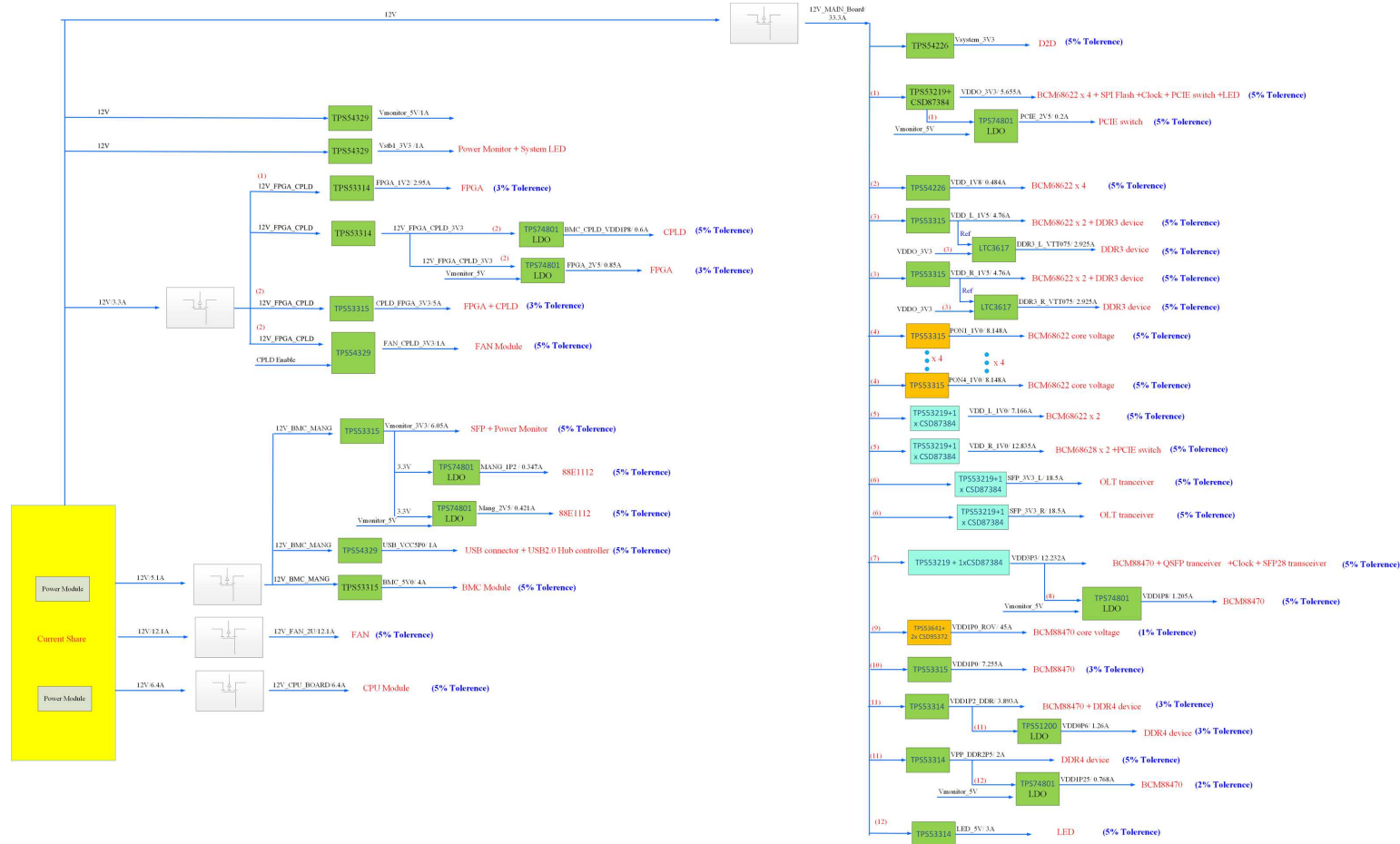
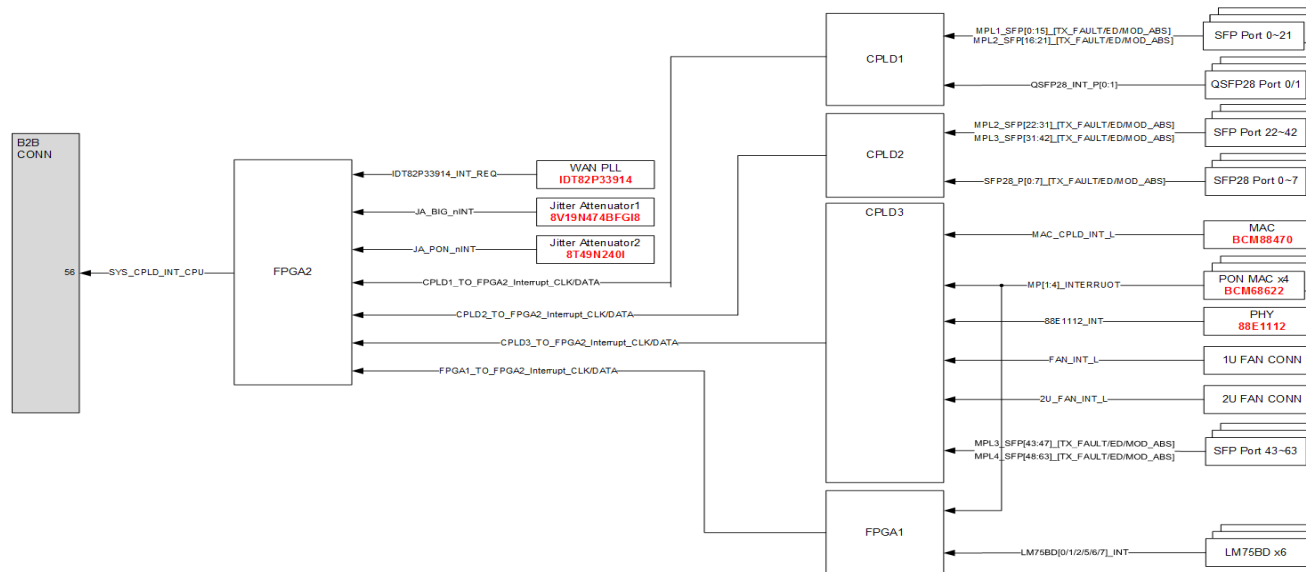
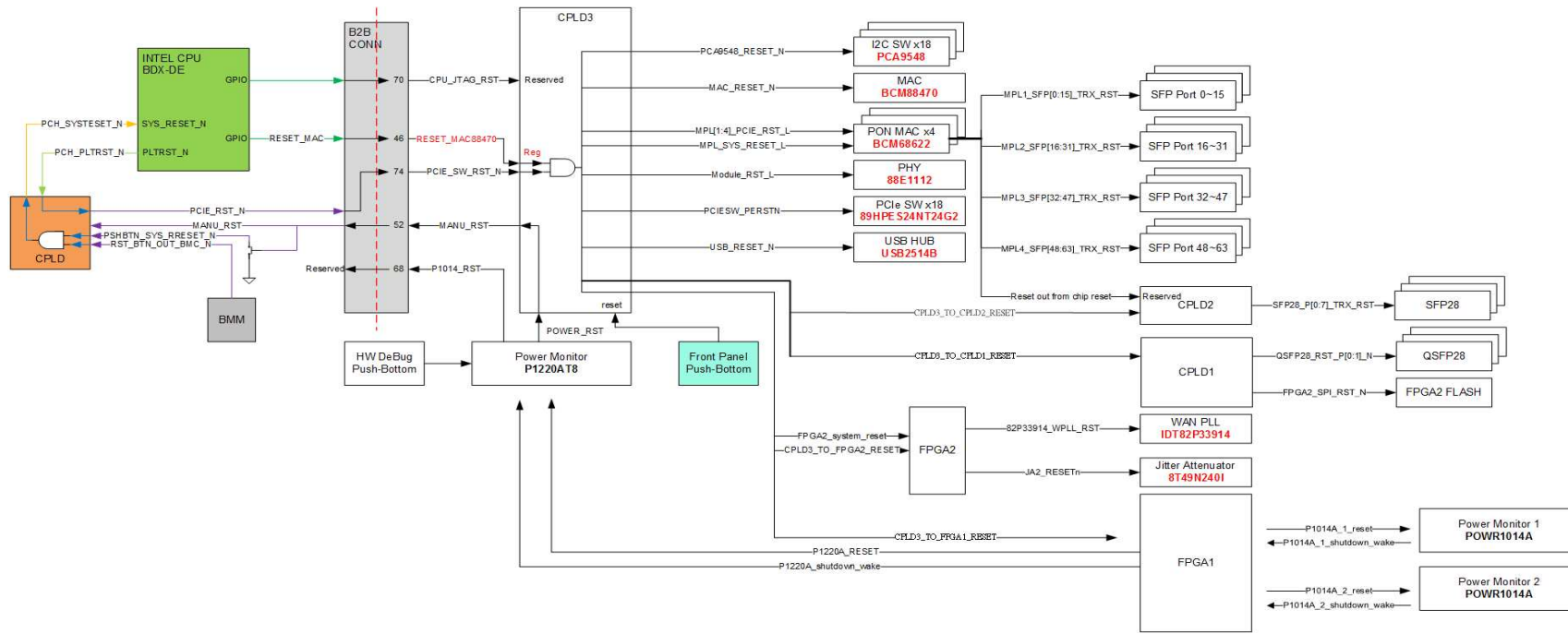


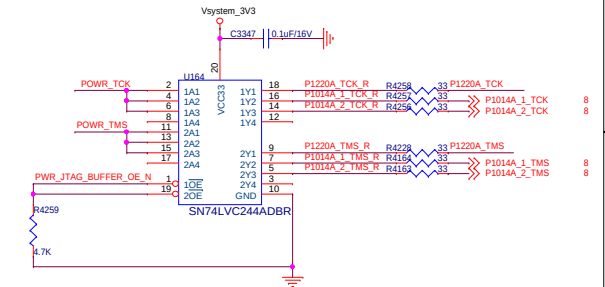
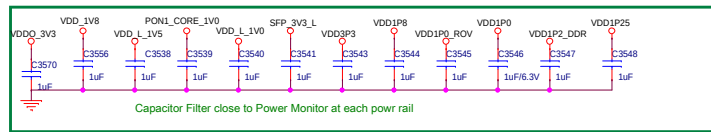
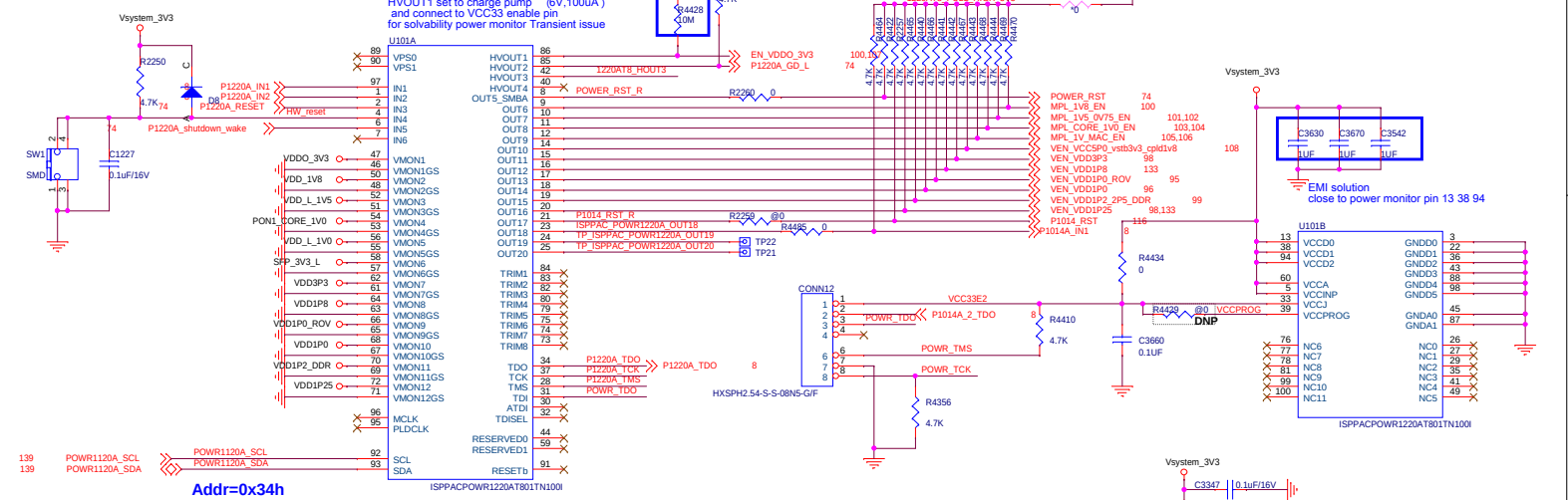


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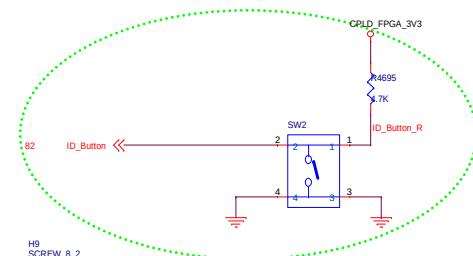
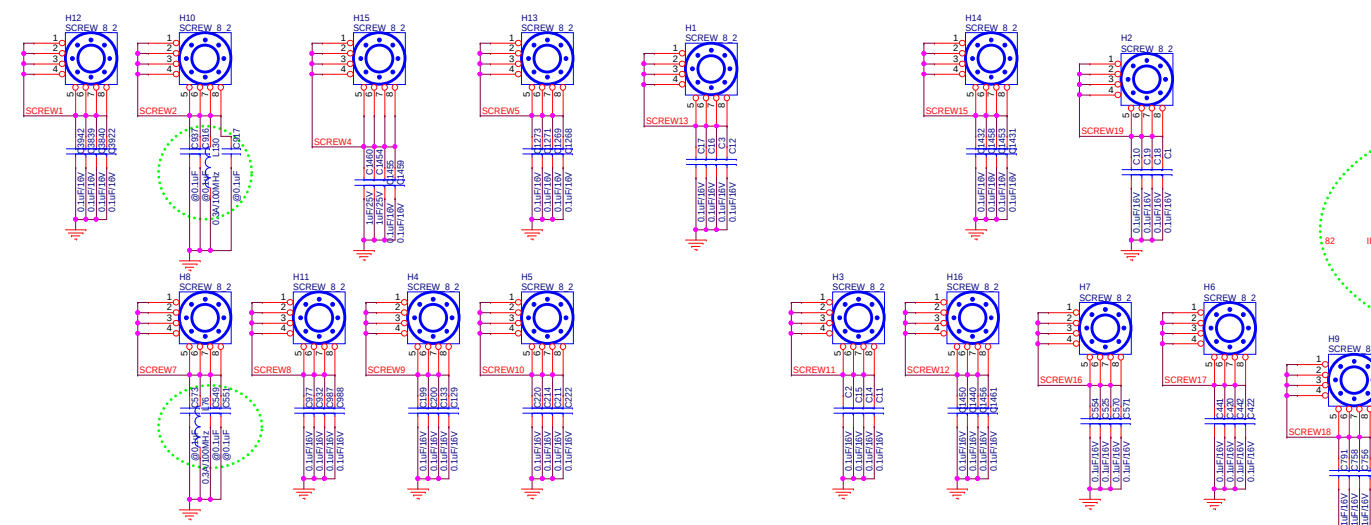


Power Controller

Vendor suggest 10M pull down
 HVOUT3 set to charge pump (6V,100uA)
 HVOUT1 set to charge pump (6V,100uA)
 and connect to VCC33 enable pin
 for solvability power monitor Transient issue



Mounting Hole



For BMC ID Button(ZZ)



[illegible]

The image shows two circuit diagrams. The left diagram shows a VDD3P3 supply connected to a resistor RA40 (1K), which is connected to a node labeled PUC5_I2C_ADD_0. This node is also connected to a resistor RA59 (1K), which is connected to ground. The right diagram shows a VDD3P3 supply connected to a resistor RA46 (1K), which is connected to a node labeled PUC6_I2C_ADD_1. This node is also connected to a resistor RA66 (1K), which is connected to ground. To the right of the diagrams, there are two red labels: '00' and '0x44'.

PLL source select should be 1 for normal operation.
When set to 1, the UC PLL is driven by the UC_PLL_REF_CLK_P/N.
When set to 0, the UC PLL is driven
by the CLOCK25, for test purposes only

1K JTAG test enable.
Must be pulled low during normal device operation.
To enable JTAG functionality, this pin must be pulled high.

This pin is used for graceful shutdown when the card is extracted and should be connected to the backplane connector for early detection of card extraction. Set to 1 for graceful shutdown. For normal operation, this pin should be pulled low.

This pin is used for graceful shutdown when the card is extracted and should be connected to the backplane connector for early detection of card extraction. Set to 1 for graceful shutdown. For normal operation, this pin should be pulled low.

RX had
internal AC
capacitors

QSFP28 Port0

QSFP28 Port1

SFP28 Port0-3

SFP28 Port4-7

QSFP28 Port0

QSFP28 Port1

SFP28 Port0-3

SFP28 Port4-7

MAPLE 1
17 18 22 23

MAPLE 2
25 26 33 34

MAPLE 3
38 39 41 43

MAPLE 4
29 30 45 46

From CPU116 10G_KR_TX1_P 10G_KR_TX1_N 10G_KR_TX0_P 10G_KR_TX0_N

From CPU116 10G_KR_TX0_P 10G_KR_TX0_N



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Model Name

GPON OLT

Rev

R0A

Size

C

Page Name

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Date:

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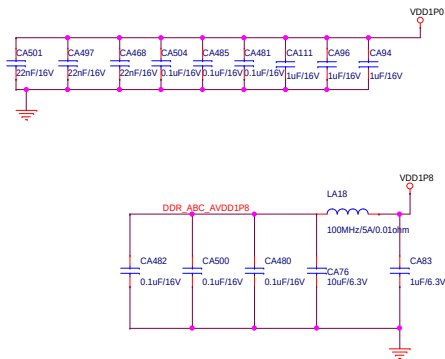
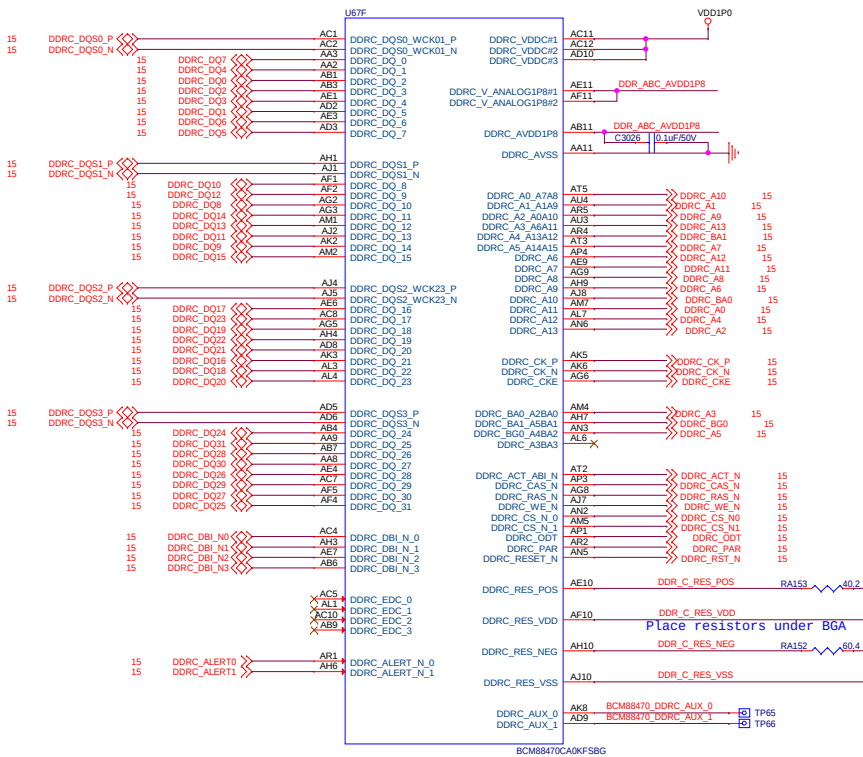
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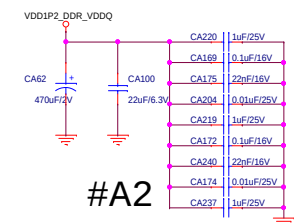
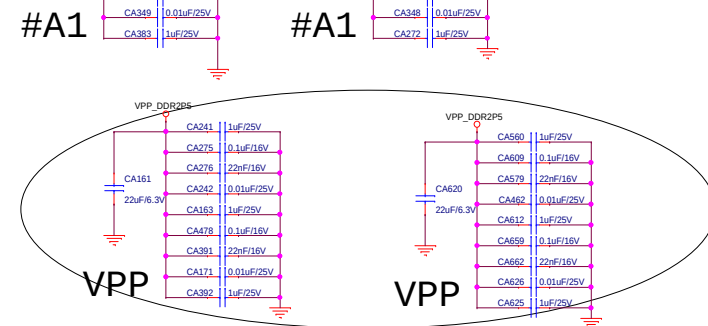
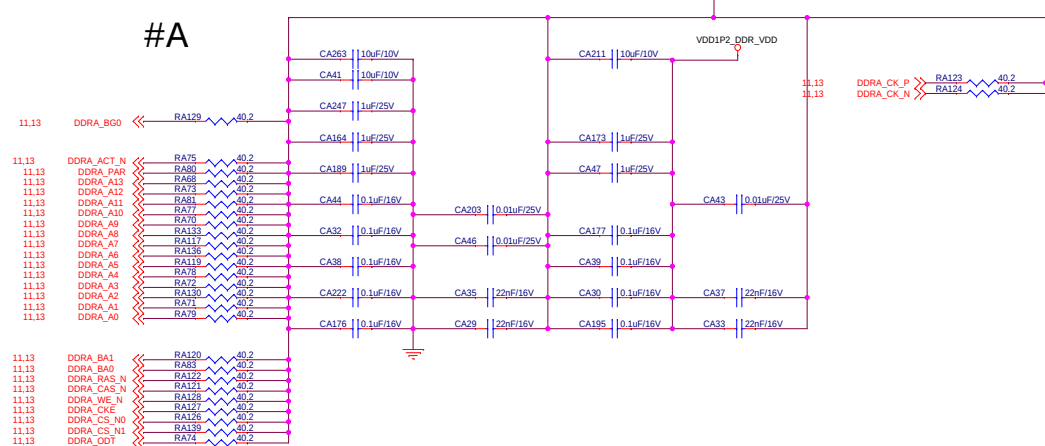
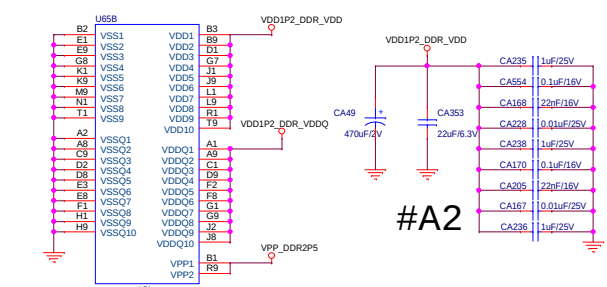
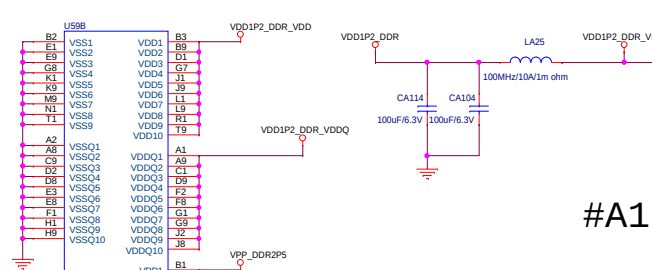
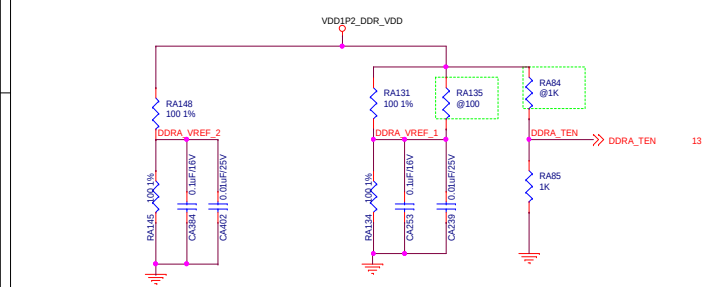
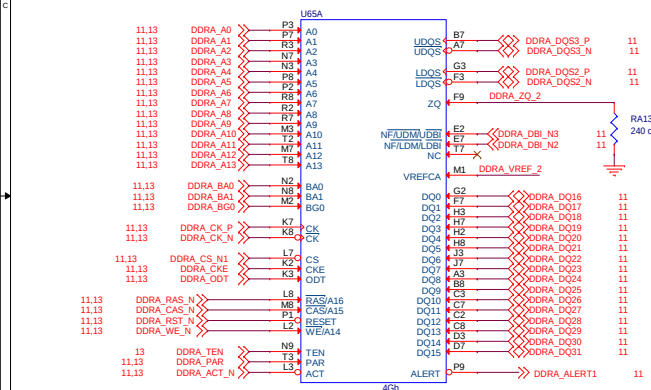
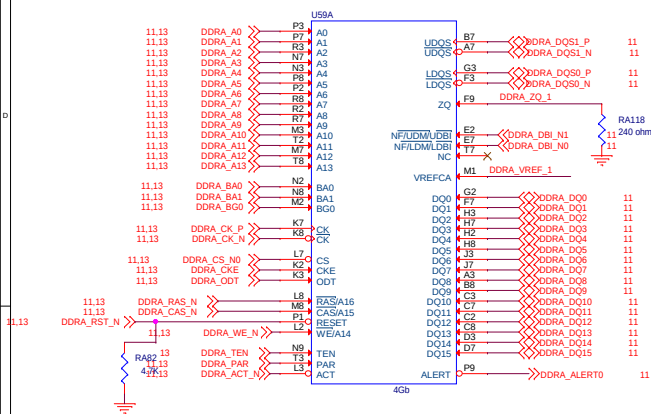
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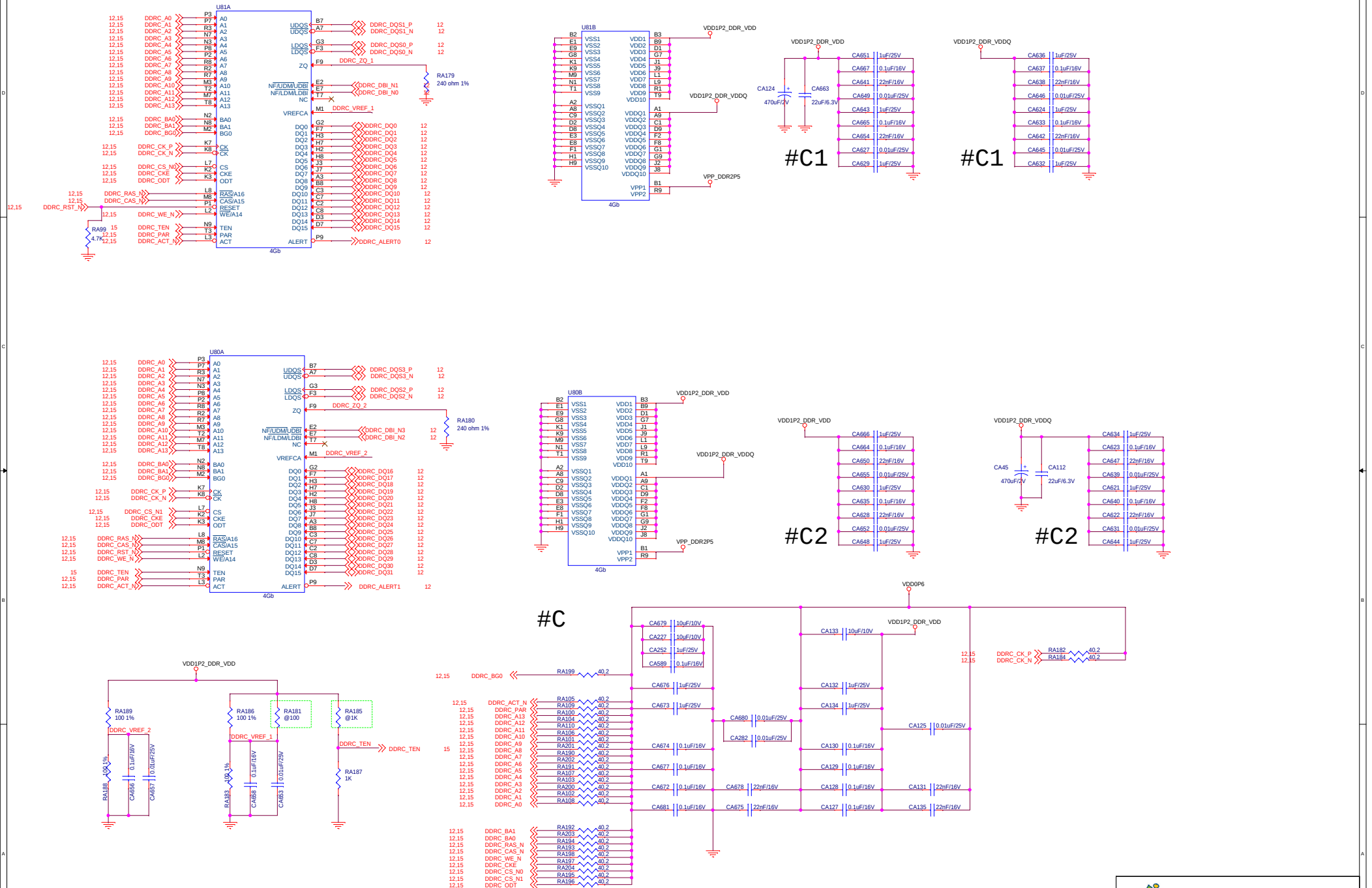


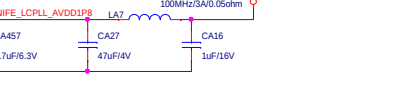
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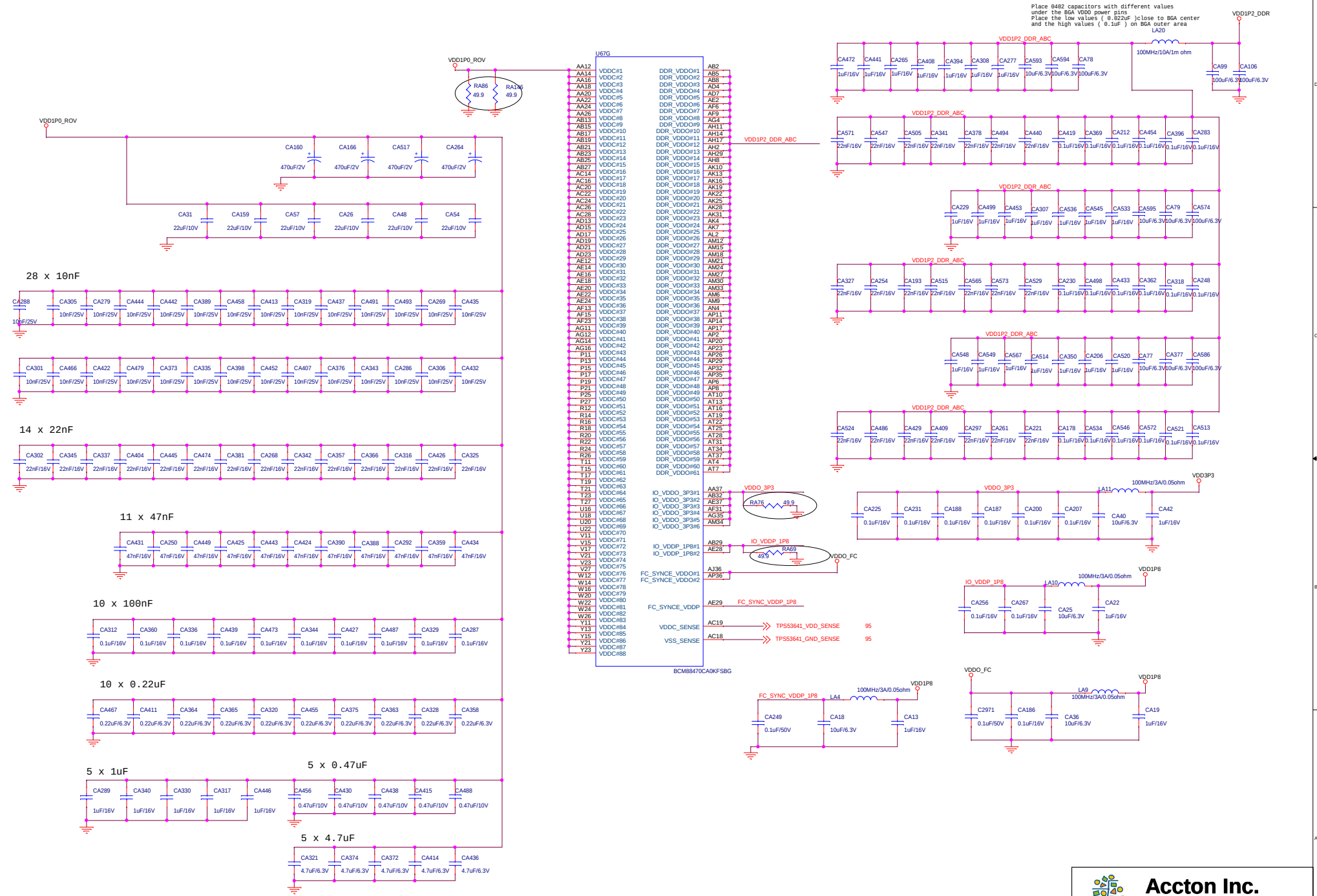
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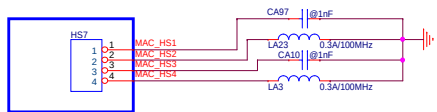
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C	DDRA				
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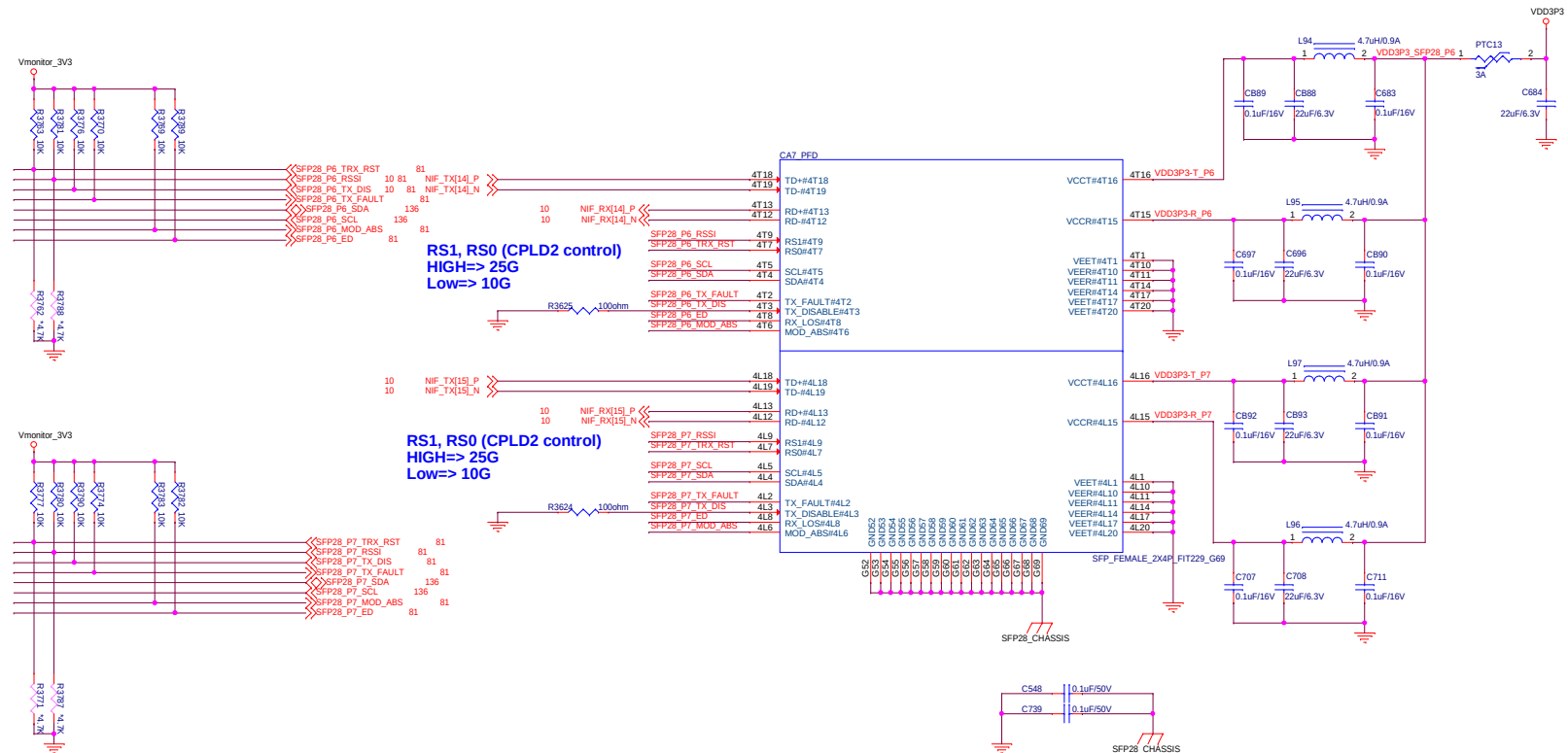
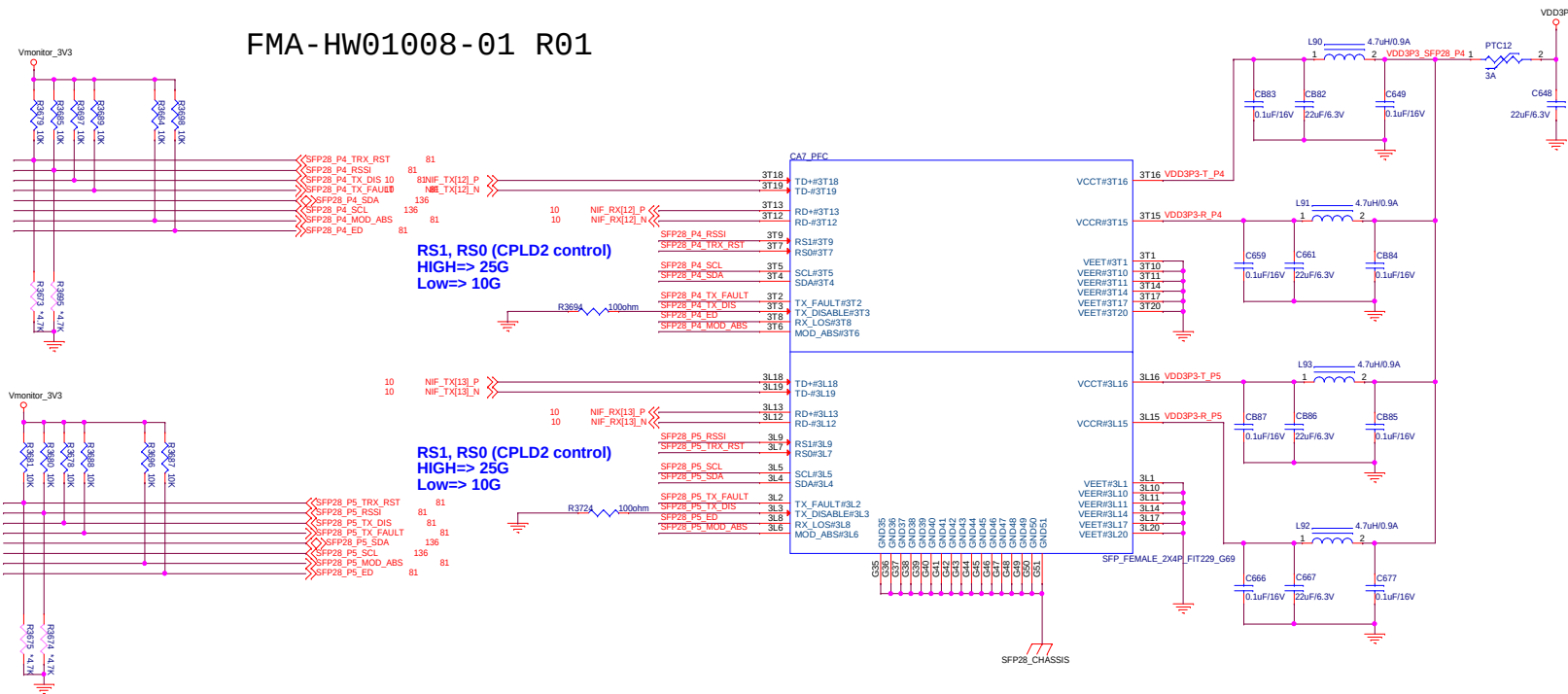




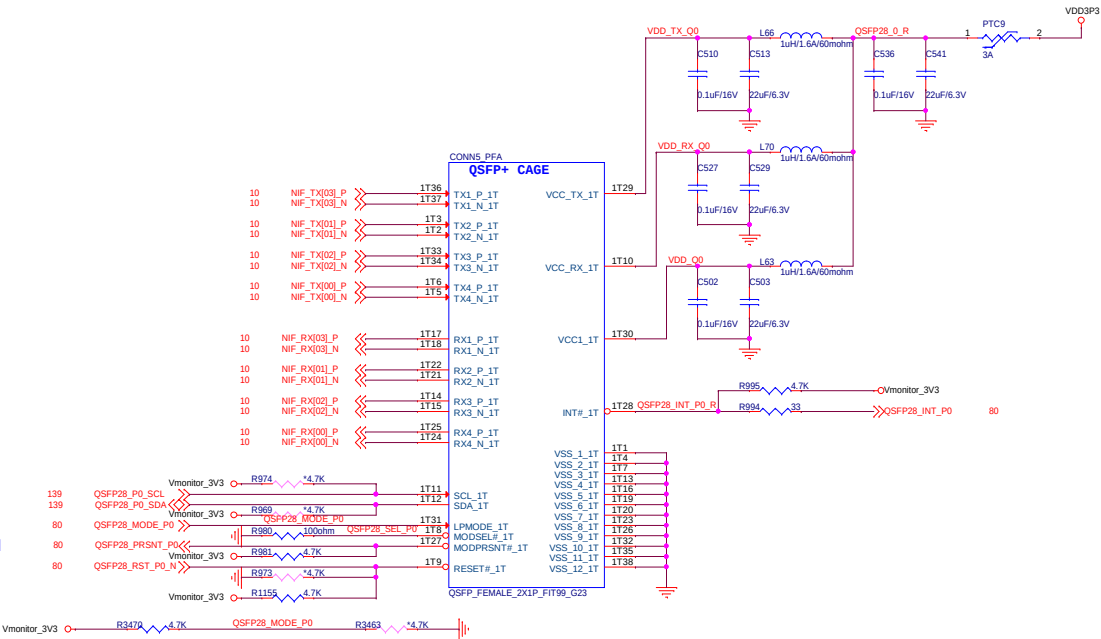


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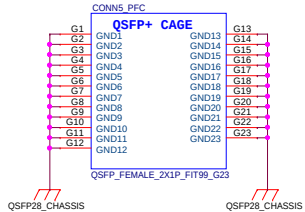
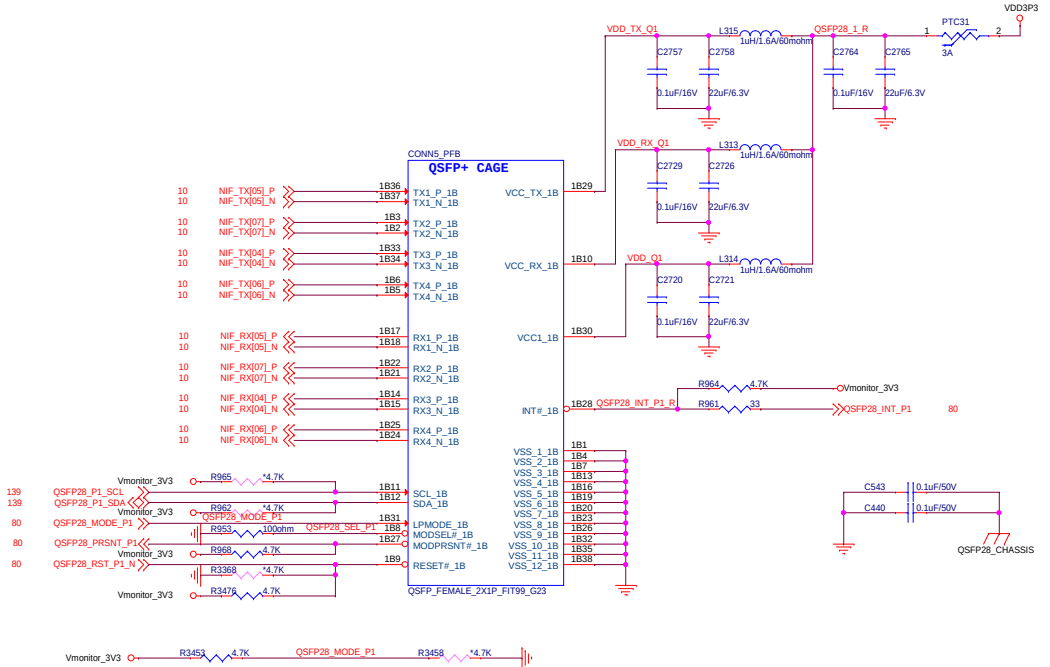
FMA-HW01008-01 R01



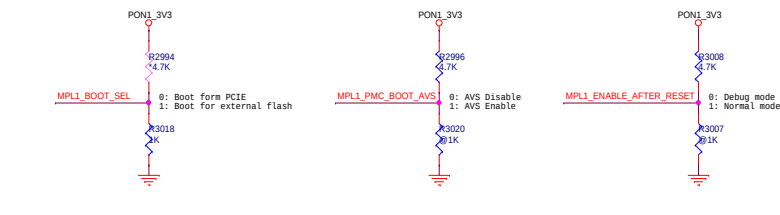
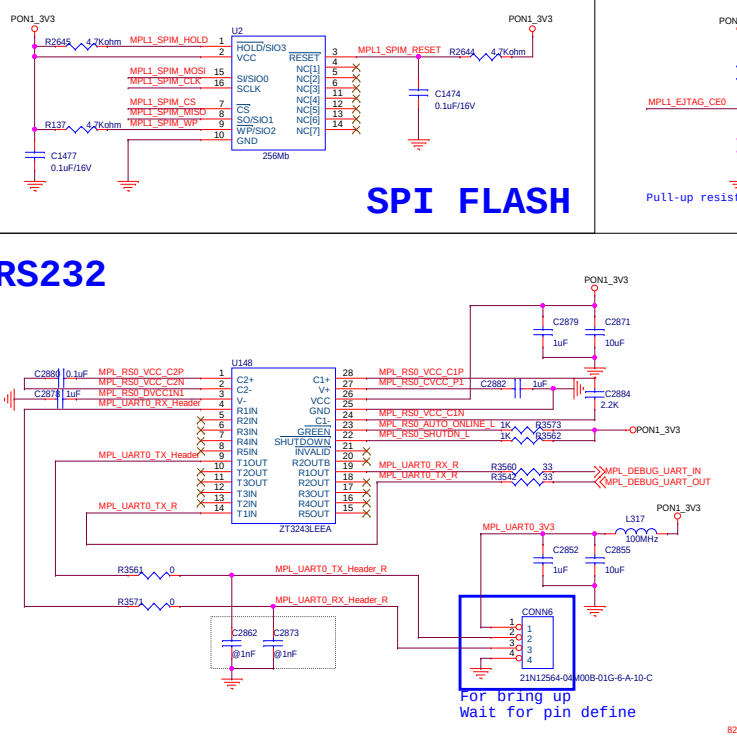
CPLD1 control



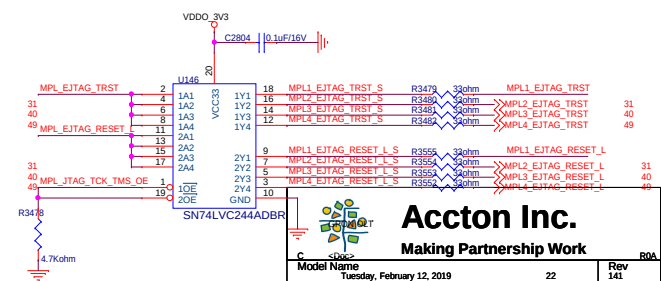
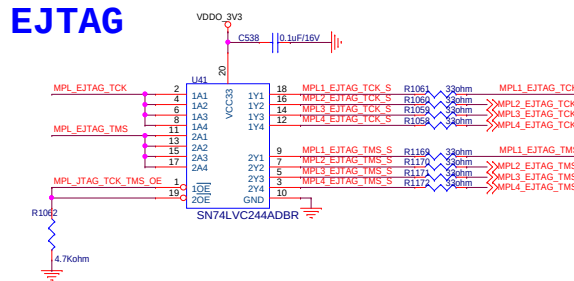
CPLD1 control

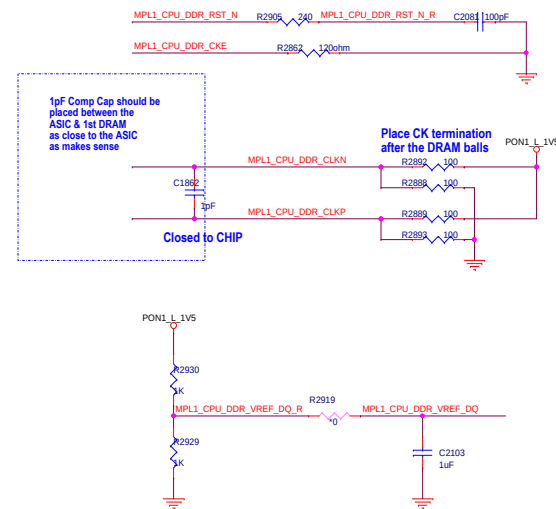
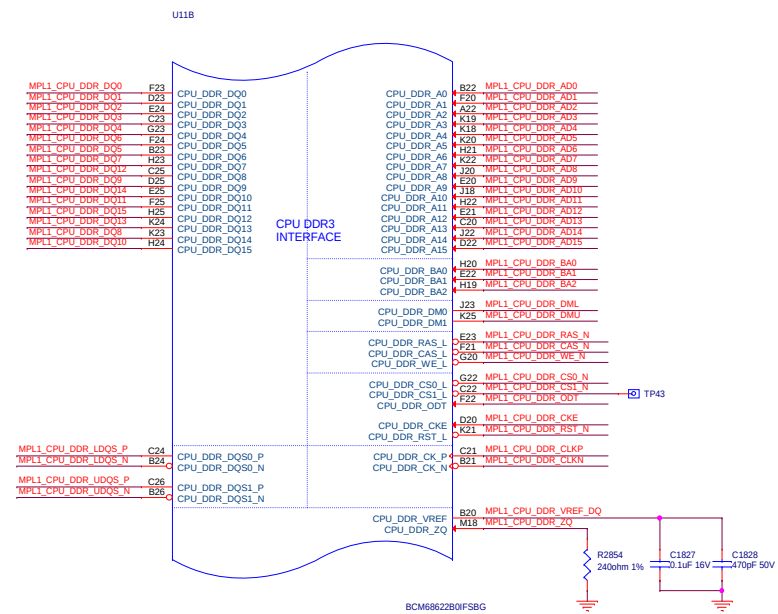


RS232

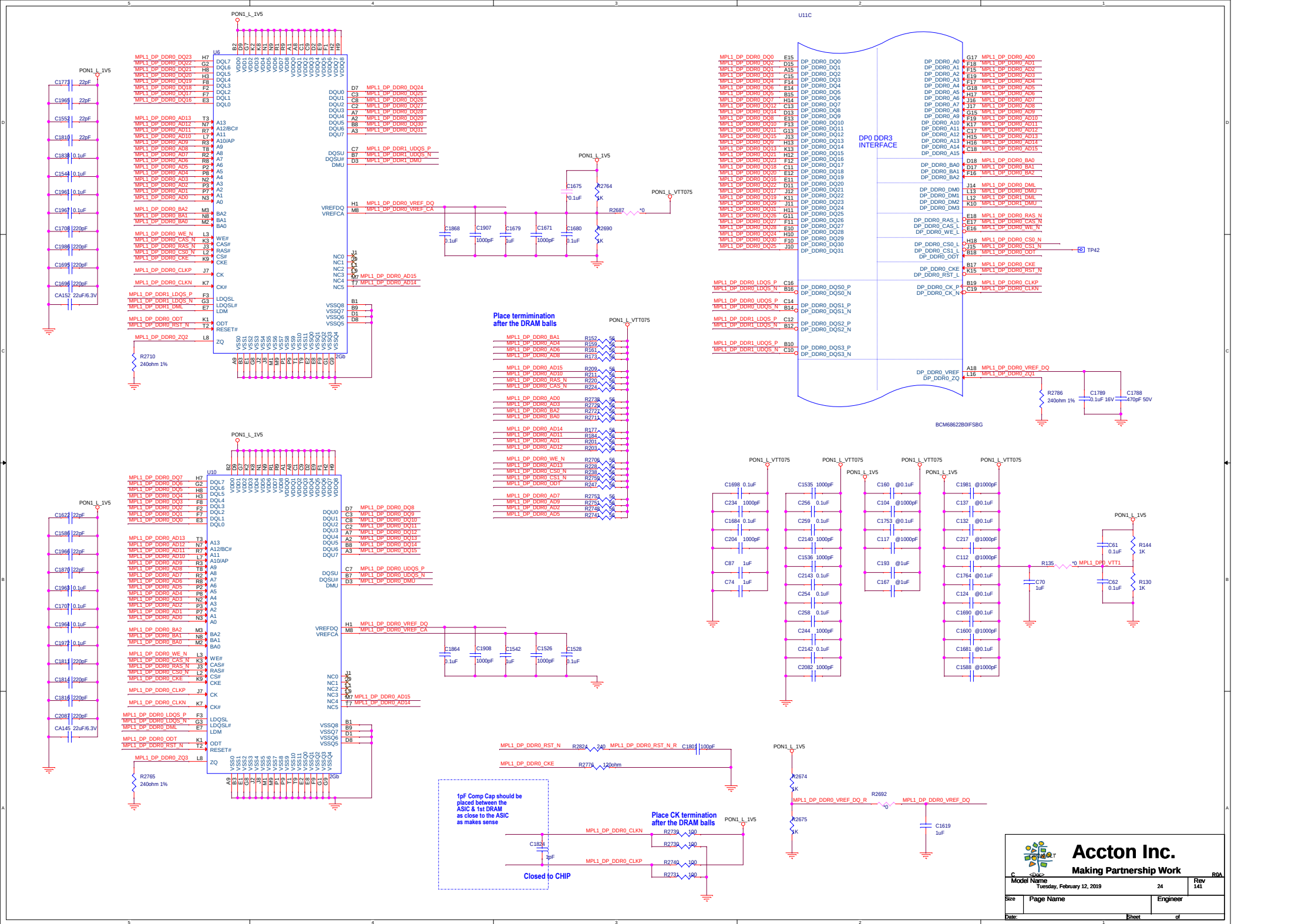


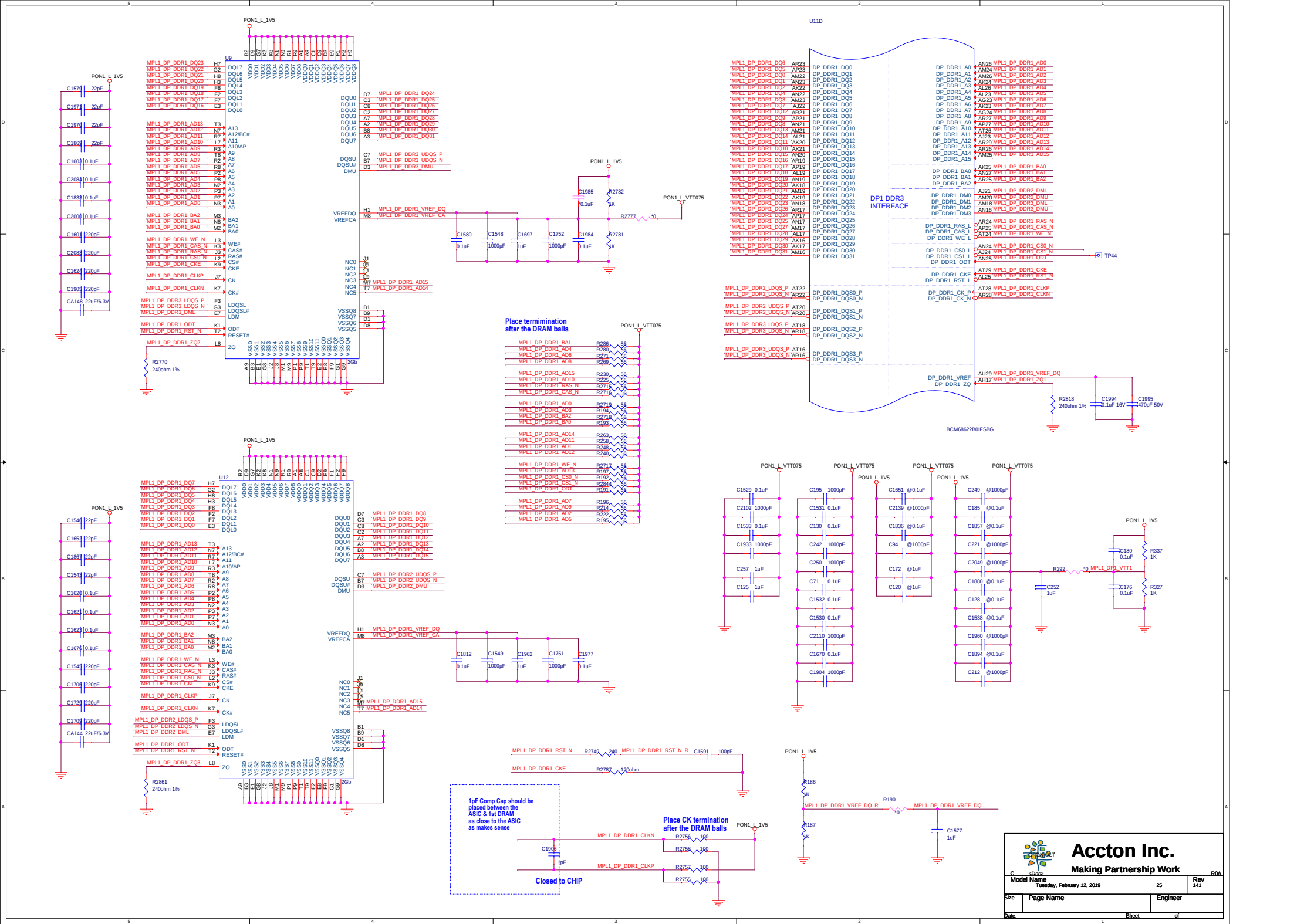
EJTAG

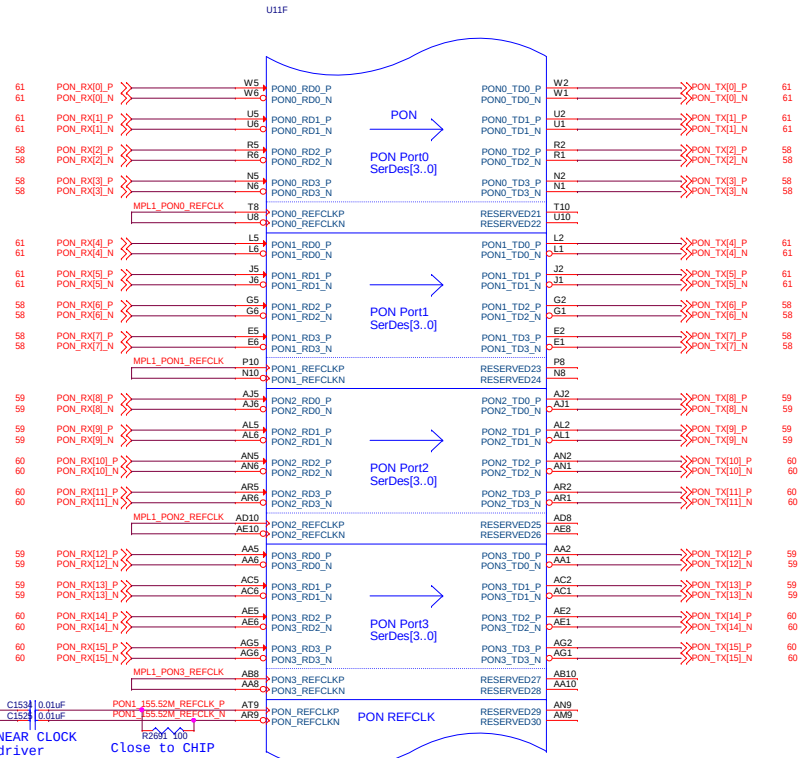




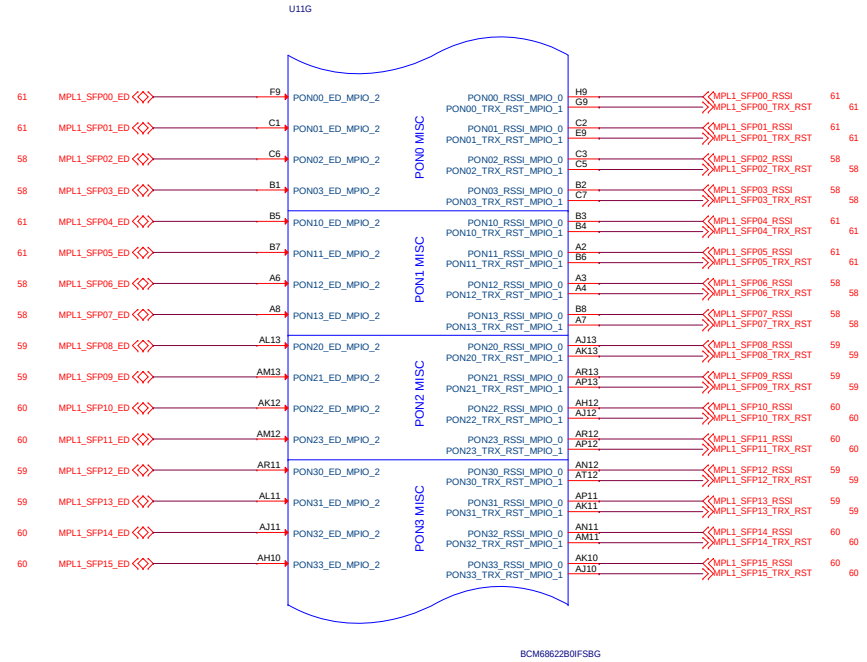
• The DDR_CLK_P/N signal from the ASIC should be routed in a fly-by from one SDRAM device to next.
 • The length of the clock trace the ASIC to DDR3-SDRAM device should be greater than or equal to the trace length of the DQS signal(s) from the ASIC to same SDRAM device.
 • The DQS, and DM signal are routed in a point-to-point fashion.
 1. The length of every trace should be matched to within 30mils to other trace within the byte group.
 2. To keep crosstalk to a minimum, keep trace separated from other trace by at least 3 times the trace width. (Typically 4 mil trace width * 3 = 12 mil keep out zone)
 • Address and control signal should be routed in a fly-by manner, like the DDR_CLK_P/N signal.
 1. The length of every trace should be matched to within 150 mils to other trace within ADD/CTRL and DDR_CLK_P/N group.
 2. Place termination to VTT after the last SDRAM balls.
 • The trace width of VTT and VREF should be 40 mils minimum.
 • Sometimes a PCB layout designer may want to swap data bits to simplify the routing of a data bus.
 For DDR3-SDRAM, it is permissible to swap data bits (though only within a byte lane).
 • Keep the maximum byte-lane group-to-byte group matched length deviation to +/- 0.2 inches.

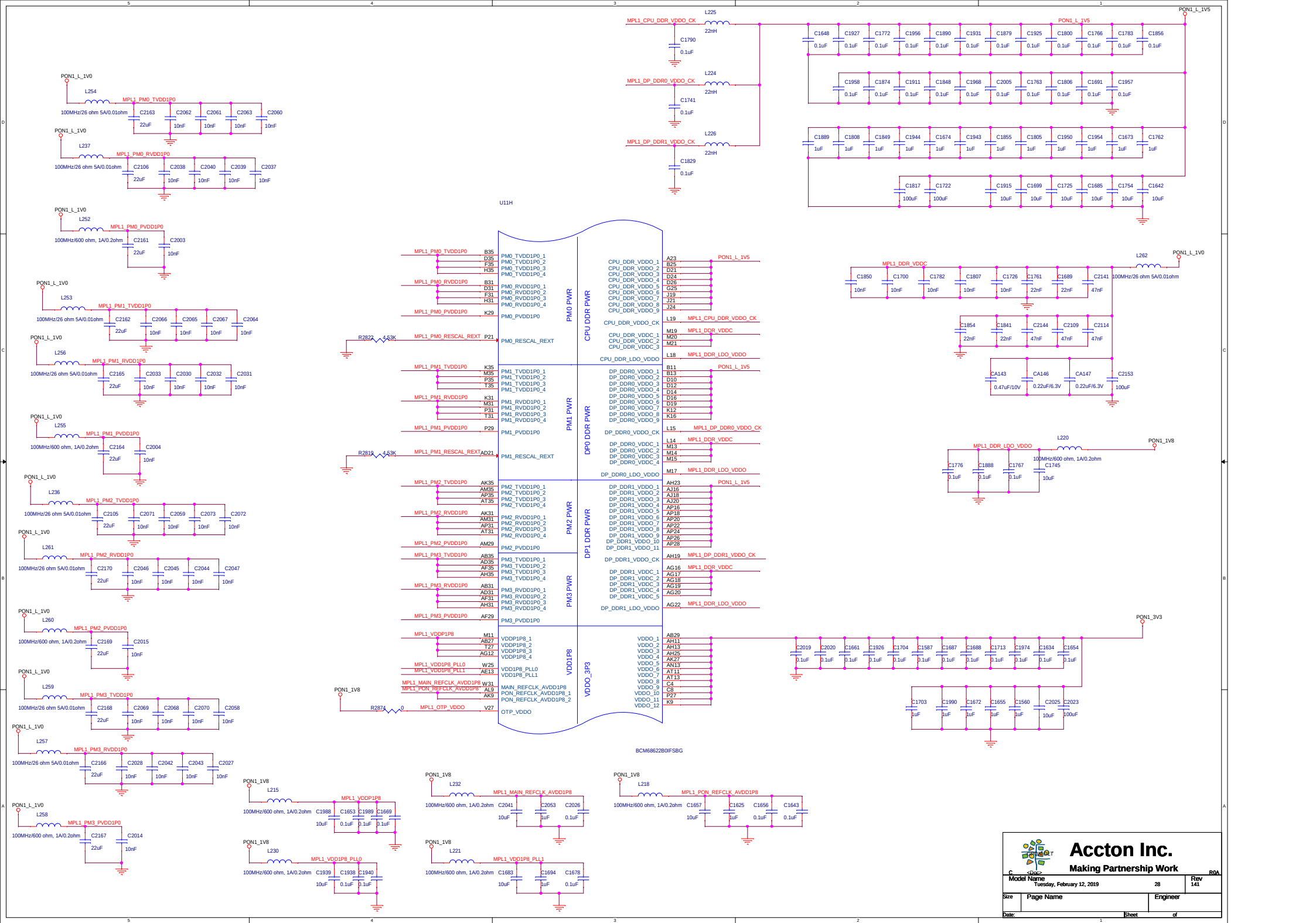






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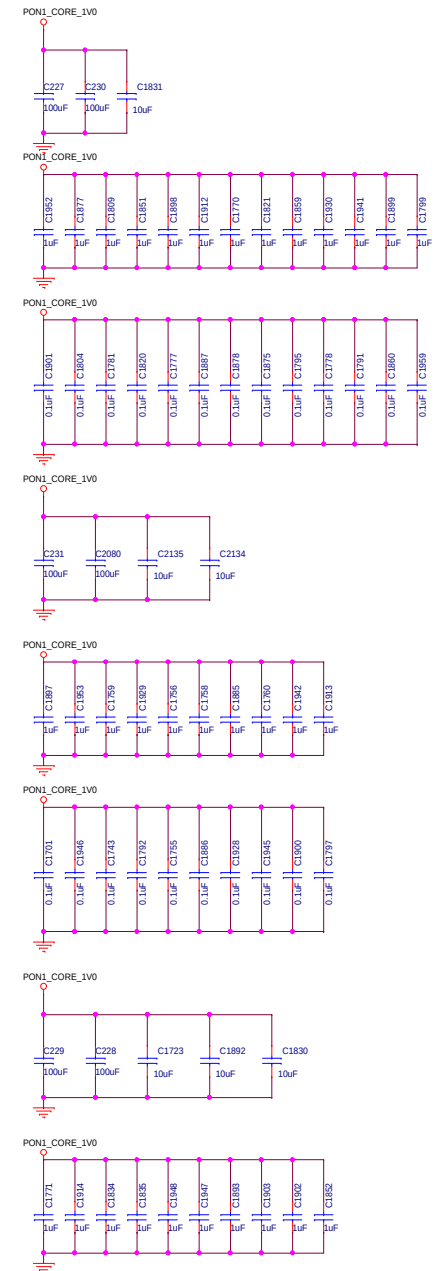
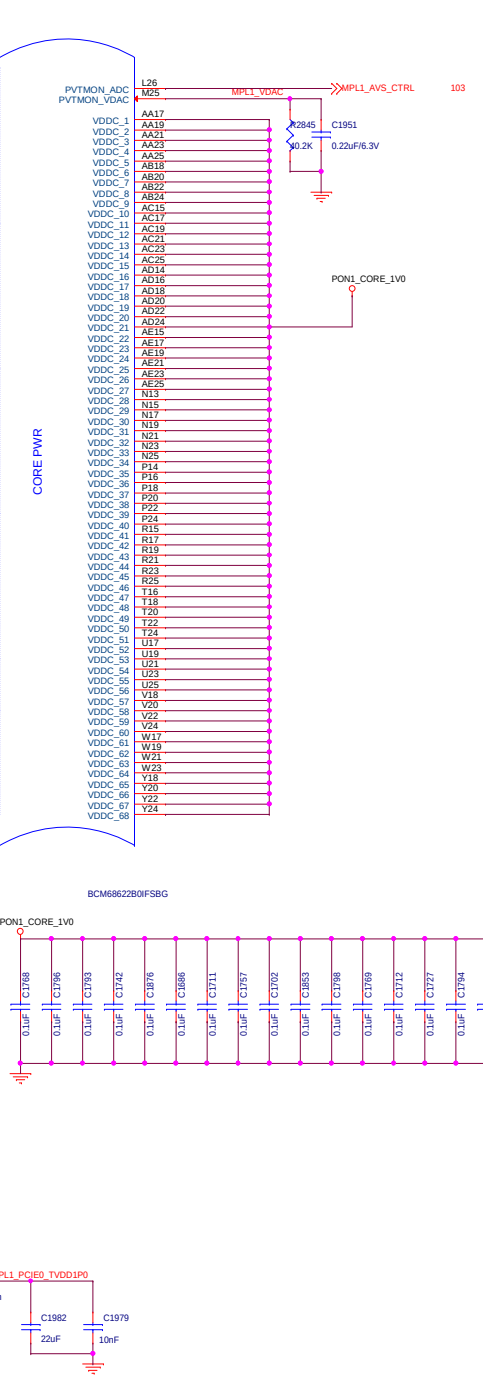
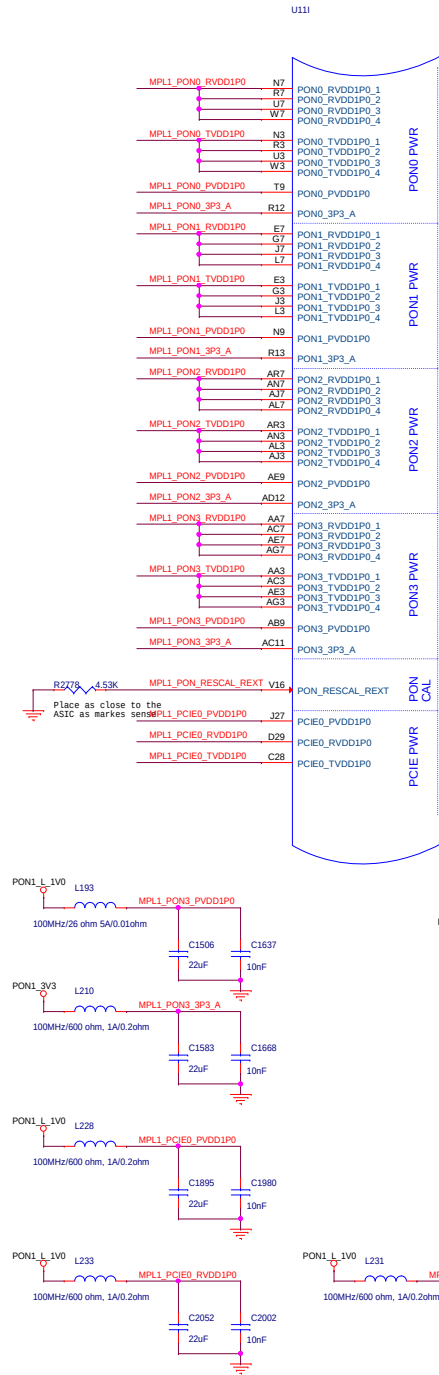
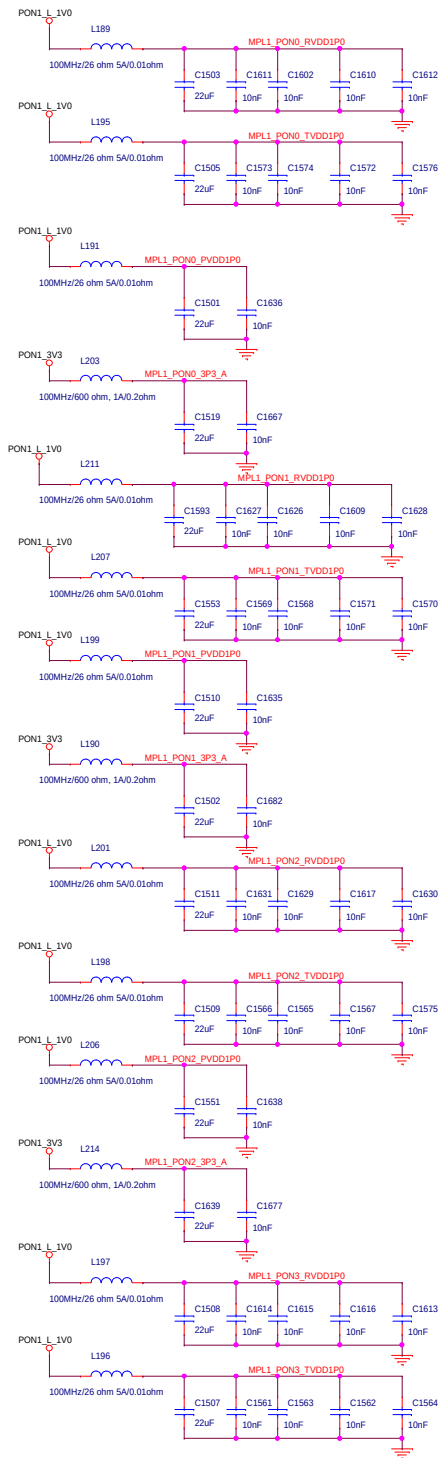




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U1L1			
A30	PM_AGN_D_1	PM_AGN_D_75	C35
A31	PM_AGN_D_2	PM_AGN_D_76	C36
A32	PM_AGN_D_3	PM_AGN_D_77	C37
A33	PM_AGN_D_4	PM_AGN_D_78	D30
A34	PM_AGN_D_5	PM_AGN_D_79	D34
A35	PM_AGN_D_6	PM_AGN_D_80	E30
A36	PM_AGN_D_7	PM_AGN_D_81	E32
A37	PM_AGN_D_8	PM_AGN_D_82	E33
AA31	PM_AGN_D_9	PM_AGN_D_83	E34
AA32	PM_AGN_D_10	PM_AGN_D_84	E35
AA33	PM_AGN_D_11	PM_AGN_D_85	E36
AA34	PM_AGN_D_12	PM_AGN_D_86	E37
AA35	PM_AGN_D_13	PM_AGN_D_87	F30
AA36	PM_AGN_D_14	PM_AGN_D_88	F31
AB30	PM_AGN_D_15	PM_AGN_D_89	G30
AB34	PM_AGN_D_16	PM_AGN_D_90	G31
AC29	PM_AGN_D_17	PM_AGN_D_91	G32
AC30	PM_AGN_D_18	PM_AGN_D_92	G33
AC31	PM_AGN_D_19	PM_AGN_D_93	G34
AC32	PM_AGN_D_20	PM_AGN_D_94	G35
AC33	PM_AGN_D_21	PM_AGN_D_95	G36
AC34	PM_AGN_D_22	PM_AGN_D_96	G37
AC35	PM_AGN_D_23	PM_AGN_D_97	H28
AC36	PM_AGN_D_24	PM_AGN_D_98	H29
AC37	PM_AGN_D_25	PM_AGN_D_99	H30
AD29	PM_AGN_D_26	PM_AGN_D_100	H34
AD30	PM_AGN_D_27	PM_AGN_D_101	I28
AD34	PM_AGN_D_28	PM_AGN_D_102	I31
AE31	PM_AGN_D_29	PM_AGN_D_103	I33
AE32	PM_AGN_D_30	PM_AGN_D_104	I34
AE33	PM_AGN_D_31	PM_AGN_D_105	I35
AE34	PM_AGN_D_32	PM_AGN_D_106	I36
AE35	PM_AGN_D_33	PM_AGN_D_107	I37
AE36	PM_AGN_D_34	PM_AGN_D_108	K28
AE37	PM_AGN_D_35	PM_AGN_D_109	K30
AF28	PM_AGN_D_36	PM_AGN_D_110	K31
AF30	PM_AGN_D_37	PM_AGN_D_111	K32
AF34	PM_AGN_D_38	PM_AGN_D_112	L28
AG31	PM_AGN_D_39	PM_AGN_D_113	L31
AG32	PM_AGN_D_40	PM_AGN_D_114	L32
AG33	PM_AGN_D_41	PM_AGN_D_115	L33
AG34	PM_AGN_D_42	PM_AGN_D_116	L34
AG35	PM_AGN_D_43	PM_AGN_D_117	L35
AG36	PM_AGN_D_44	PM_AGN_D_118	L36
AG37	PM_AGN_D_45	PM_AGN_D_119	L37
AH29	PM_AGN_D_46	PM_AGN_D_120	M28
AH30	PM_AGN_D_47	PM_AGN_D_121	M29
AH34	PM_AGN_D_48	PM_AGN_D_122	M30
AJ29	PM_AGN_D_49	PM_AGN_D_123	M34
AJ30	PM_AGN_D_50	PM_AGN_D_124	N31
AJ31	PM_AGN_D_51	PM_AGN_D_125	N32
AJ32	PM_AGN_D_52	PM_AGN_D_126	N33
AJ33	PM_AGN_D_53	PM_AGN_D_127	N34
AJ34	PM_AGN_D_54	PM_AGN_D_128	N35
AJ35	PM_AGN_D_55	PM_AGN_D_129	N36
AJ36	PM_AGN_D_56	PM_AGN_D_130	N37
AK29	PM_AGN_D_57	PM_AGN_D_131	P28
AK30	PM_AGN_D_58	PM_AGN_D_132	P30
AK34	PM_AGN_D_59	PM_AGN_D_133	P34
AL31	PM_AGN_D_60	PM_AGN_D_134	P35
AL32	PM_AGN_D_61	PM_AGN_D_135	R32
AL33	PM_AGN_D_62	PM_AGN_D_136	R33
AL34	PM_AGN_D_63	PM_AGN_D_137	R34
AL35	PM_AGN_D_64	PM_AGN_D_138	R35
AL36	PM_AGN_D_65	PM_AGN_D_139	R36
AL37	PM_AGN_D_66	PM_AGN_D_140	R37
AM28	PM_AGN_D_67	PM_AGN_D_141	T29
AM30	PM_AGN_D_68	PM_AGN_D_142	T30
AM34	PM_AGN_D_69	PM_AGN_D_143	T34
AN24	PM_AGN_D_70	PM_AGN_D_144	U31
AN31	PM_AGN_D_71	PM_AGN_D_145	U32
AN32	PM_AGN_D_72	PM_AGN_D_146	U33
AN33	PM_AGN_D_73	PM_AGN_D_147	U34
	PM_AGN_D_74	PM_AGN_D_148	U35

AA31	PON_AGN_D_64	PON_AGN_D_138	AJ5
AA35	PON_AGN_D_65	PON_AGN_D_139	AJ6
AA41	PON_AGN_D_66	PON_AGN_D_140	AJ7
AA9	PON_AGN_D_67	PON_AGN_D_141	AJ8
AB1	PON_AGN_D_68	PON_AGN_D_142	D2
AB11	PON_AGN_D_69	PON_AGN_D_143	D3
AB14	PON_AGN_D_70	PON_AGN_D_144	D4
AB15	PON_AGN_D_71	PON_AGN_D_145	D5
AB5	PON_AGN_D_72	PON_AGN_D_146	D6
AB3	PON_AGN_D_73	PON_AGN_D_147	D7
AB7	PON_AGN_D_74	PON_AGN_D_148	D8
AB31	PON_AGN_D_75	PON_AGN_D_149	E4
AB35	PON_AGN_D_76	PON_AGN_D_150	E5
AB6	PON_AGN_D_77	PON_AGN_D_151	F1
AC13	PON_AGN_D_78	PON_AGN_D_152	F2
AC10	PON_AGN_D_79	PON_AGN_D_153	F3
AC12	PON_AGN_D_80	PON_AGN_D_154	F4
AC1	PON_AGN_D_81	PON_AGN_D_155	F5
AC8	PON_AGN_D_82	PON_AGN_D_156	F6
AC3	PON_AGN_D_83	PON_AGN_D_157	F7
AD1	PON_AGN_D_84	PON_AGN_D_158	F8
AD11	PON_AGN_D_85	PON_AGN_D_159	G4
AD3	PON_AGN_D_86	PON_AGN_D_160	G5
AD4	PON_AGN_D_87	PON_AGN_D_161	G8
AD6	PON_AGN_D_88	PON_AGN_D_162	H2
AD7	PON_AGN_D_89	PON_AGN_D_163	H3
AD9	PON_AGN_D_90	PON_AGN_D_164	H4
AE11	PON_AGN_D_91	PON_AGN_D_165	H5
AE4	PON_AGN_D_92	PON_AGN_D_166	H8
AF1	PON_AGN_D_93	PON_AGN_D_167	H9
AF2	PON_AGN_D_94	PON_AGN_D_168	H8
AF3	PON_AGN_D_95	PON_AGN_D_169	H8
AF4	PON_AGN_D_96	PON_AGN_D_170	K1
AF5	PON_AGN_D_97	PON_AGN_D_171	K2
AF6	PON_AGN_D_98	PON_AGN_D_172	K3
AF7	PON_AGN_D_99	PON_AGN_D_173	K4
AF8	PON_AGN_D_100	PON_AGN_D_174	K5
AF9	PON_AGN_D_101	PON_AGN_D_175	K6
AG1	PON_AGN_D_102	PON_AGN_D_176	K7
AG2	PON_AGN_D_103	PON_AGN_D_177	K8
AG3	PON_AGN_D_104	PON_AGN_D_178	K9
AG4	PON_AGN_D_105	PON_AGN_D_179	L4
AG5	PON_AGN_D_106	PON_AGN_D_180	L8
AG9	PON_AGN_D_107	PON_AGN_D_181	L9
AH1	PON_AGN_D_108	PON_AGN_D_182	M0
AH2	PON_AGN_D_109	PON_AGN_D_183	M1
AH3	PON_AGN_D_110	PON_AGN_D_184	M2
AH4	PON_AGN_D_111	PON_AGN_D_185	M3
AH5	PON_AGN_D_112	PON_AGN_D_186	M4
AH6	PON_AGN_D_113	PON_AGN_D_187	M5
AH7	PON_AGN_D_114	PON_AGN_D_188	M6
AH8	PON_AGN_D_115	PON_AGN_D_189	M7
AJ1	PON_AGN_D_116	PON_AGN_D_190	M8
AJ3	PON_AGN_D_117	PON_AGN_D_191	M9
AJ4	PON_AGN_D_118	PON_AGN_D_192	N11
AJ5	PON_AGN_D_119	PON_AGN_D_193	N14
AJ6	PON_AGN_D_120	PON_AGN_D_194	P1
AJ7	PON_AGN_D_121	PON_AGN_D_195	P11
AJ8	PON_AGN_D_122	PON_AGN_D_196	P12
AJ9	PON_AGN_D_123	PON_AGN_D_197	P2
AK1	PON_AGN_D_124	PON_AGN_D_198	P3
AK2	PON_AGN_D_125	PON_AGN_D_199	P4
AK3	PON_AGN_D_126	PON_AGN_D_200	P5
AK4	PON_AGN_D_127	PON_AGN_D_201	P6
AK5	PON_AGN_D_128	PON_AGN_D_202	P7
AK6	PON_AGN_D_129	PON_AGN_D_203	P9
AK7	PON_AGN_D_130	PON_AGN_D_204	R3
AK8	PON_AGN_D_131	PON_AGN_D_205	R11
AK9	PON_AGN_D_132	PON_AGN_D_206	R4
AM1	PON_AGN_D_133	PON_AGN_D_207	R8
AM2	PON_AGN_D_134	PON_AGN_D_208	R9
AM3	PON_AGN_D_135	PON_AGN_D_209	T1
AM4	PON_AGN_D_136	PON_AGN_D_210	T11
AM5	PON_AGN_D_137	PON_AGN_D_211	T1

A1	VSS_1	VSS_69	AN8
A10	VSS_2	VSS_70	AN9
A12	VSS_3	VSS_71	AP15
A14	VSS_4	VSS_72	AP16
A16	VSS_5	VSS_73	AR10
A19	VSS_6	VSS_74	AR14
A21	VSS_7	VSS_75	AR15
A24	VSS_8	VSS_76	AT10
A26	VSS_9	VSS_77	AT15
A27	VSS_10	VSS_78	AU12
A29	VSS_11	VSS_79	AU15
A3	VSS_12	VSS_80	AM27
A9	VSS_13	VSS_81	AU16
AA18	VSS_14	VSS_82	AU18
AA20	VSS_15	VSS_83	AU20
AA22	VSS_16	VSS_84	AU22
AA24	VSS_17	VSS_85	AU24
AB17	VSS_18	VSS_86	AU28
AB19	VSS_19	VSS_87	AT25
AB21	VSS_20	VSS_88	B27
AB23	VSS_21	VSS_89	C27
AB25	VSS_22	VSS_90	C27
AB28	VSS_23	VSS_91	C9
AC16	VSS_24	VSS_92	D27
AC18	VSS_25	VSS_93	D28
AC20	VSS_26	VSS_94	D9
AC22	VSS_27	VSS_95	E29
AC24	VSS_28	VSS_96	F24
AD15	VSS_29	VSS_97	F27
AD17	VSS_30	VSS_98	F29
AD19	VSS_31	VSS_99	F29
AD25	VSS_32	VSS_100	G10
AE14	VSS_33	VSS_101	G14
AE16	VSS_34	VSS_102	G14
AE18	VSS_35	VSS_103	G16
AE20	VSS_36	VSS_104	G16
AE22	VSS_37	VSS_105	G21
AE24	VSS_38	VSS_106	G28
AE28	VSS_39	VSS_107	G28
AG13	VSS_40	VSS_108	H25
AG14	VSS_41	VSS_109	J26
AG15	VSS_42	VSS_110	J9
AG21	VSS_43	VSS_111	K14
AG26	VSS_44	VSS_112	K26
AH15	VSS_45	VSS_113	K27
AH16	VSS_46	VSS_114	L10
AH18	VSS_47	VSS_115	L11
AH20	VSS_48	VSS_116	L17
AH21	VSS_49	VSS_117	L21
AH22	VSS_50	VSS_118	M12
AH24	VSS_51	VSS_119	M16
AJ15	VSS_52	VSS_120	M25
AJ17	VSS_53	VSS_121	M24
AJ19	VSS_54	VSS_122	N12
AJ25	VSS_55	VSS_123	N12
AK15	VSS_56	VSS_124	N16
AK26	VSS_57	VSS_125	N18
AL10	VSS_58	VSS_126	N20
AL12	VSS_59	VSS_127	N22
AL16	VSS_60	VSS_128	N24
AL18	VSS_61	VSS_129	P13
AL20	VSS_62	VSS_130	P15
AL22	VSS_63	VSS_131	P17
AL24	VSS_64	VSS_132	P19
AL28	VSS_65	VSS_133	P25
AM10	VSS_66	VSS_134	R14
AM15	VSS_67	VSS_135	R16
AM15	VSS_68	VSS_136	R18
		VSS_137	R20
		VSS_138	R22
		VSS_140	R24

AF13	VSS_141	VSS_170	AD23
AF14	VSS_142	VSS_171	AC14
AF15	VSS_143	VSS_172	AB16
AF16	VSS_144	VSS_173	A20
AF17	VSS_145	VSS_174	A17
AF18	VSS_146	VSS_175	A11
AF19	VSS_147	VSS_176	A11
AF20	VSS_148	VSS_177	G24
AF21	VSS_149	VSS_178	A19
AF22	VSS_150	VSS_179	L20
AF23	VSS_151	VSS_180	L21
AF24	VSS_152	VSS_181	L22
AM27	VSS_153	VSS_182	L23
AU18	VSS_154	VSS_183	L24
AU19	VSS_155	VSS_184	L25
AU20	VSS_156	VSS_185	M22
AU21	VSS_157	VSS_186	M22
AU22	VSS_158	VSS_187	T15
AU23	VSS_159	VSS_188	T15
AU24	VSS_160	VSS_189	T17
AU25	VSS_161	VSS_190	T21
AU26	VSS_162	VSS_191	T23
AU27	VSS_163	VSS_192	T23
AU28	VSS_164	VSS_193	U16
AU29	VSS_165	VSS_194	U19
AU30	VSS_166	VSS_195	U19
AU31	VSS_167	VSS_196	U22
AU32	VSS_168	VSS_197	U24
AU33	VSS_169	VSS_198	U27
		VSS_200	V15
		VSS_201	V21
		VSS_202	V23
		VSS_203	V25
		VSS_204	W18
		VSS_205	W20
		VSS_206	W22
		VSS_207	W24
		VSS_208	V17
		VSS_209	V15
		VSS_210	V21
		VSS_211	V23
		VSS_212	V23
		VSS_213	V25

OTDR_RX_AVSS_1
OTDR_RX_AVSS_2
OTDR_RX_AVSS_3

BCM6862280F5BG

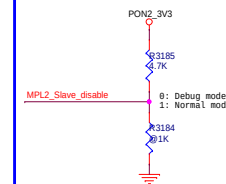
NC1
NC2
NC3
NC4
BLACK



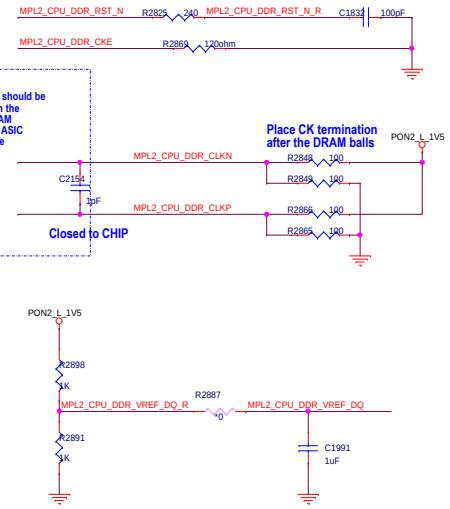
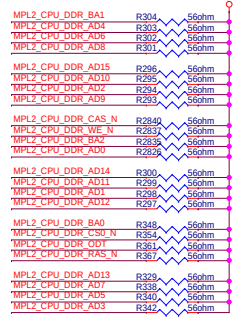
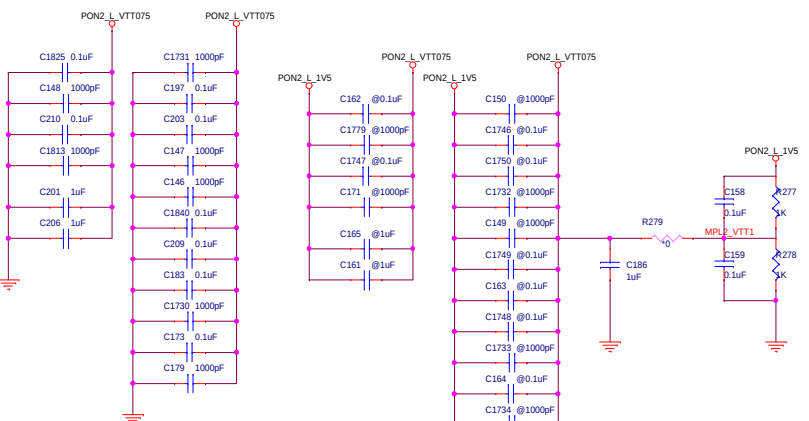
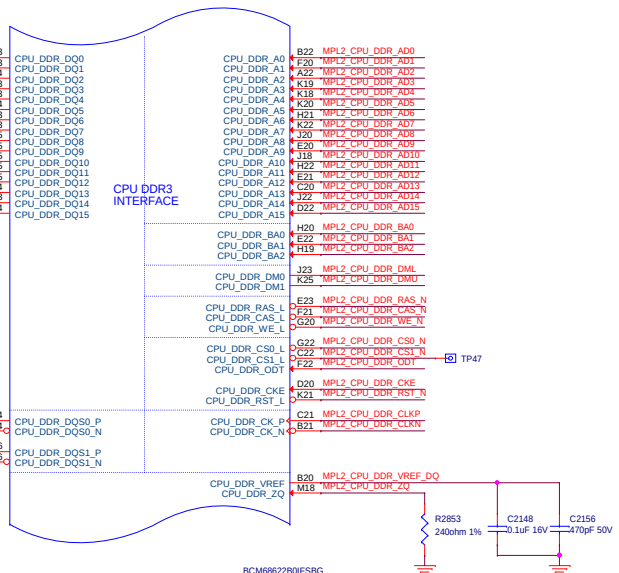
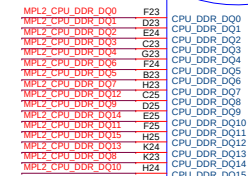
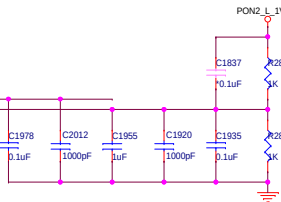
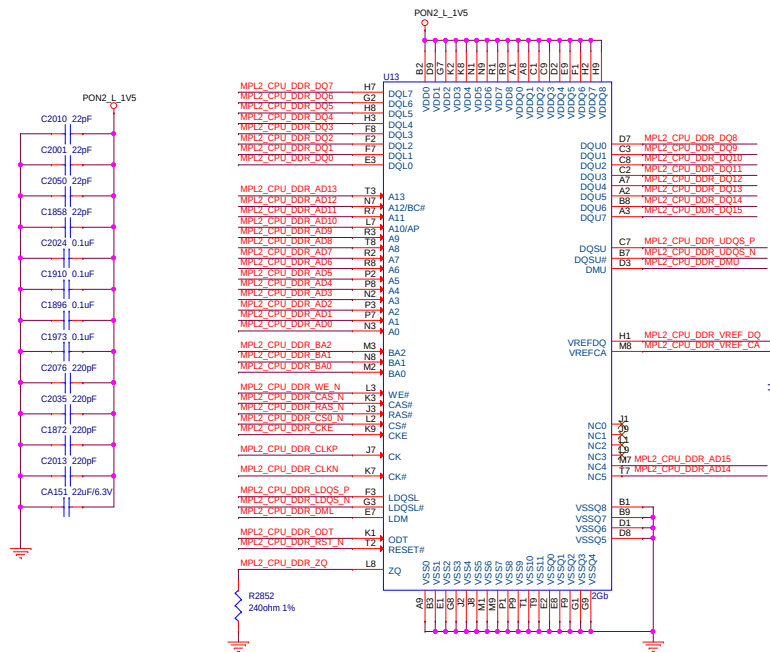
Accton Inc.

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Model Name Tuesday, February 12, 2019		30	Rev 141
Size	Page Name	Engineer	
Date:	Sheet	of	

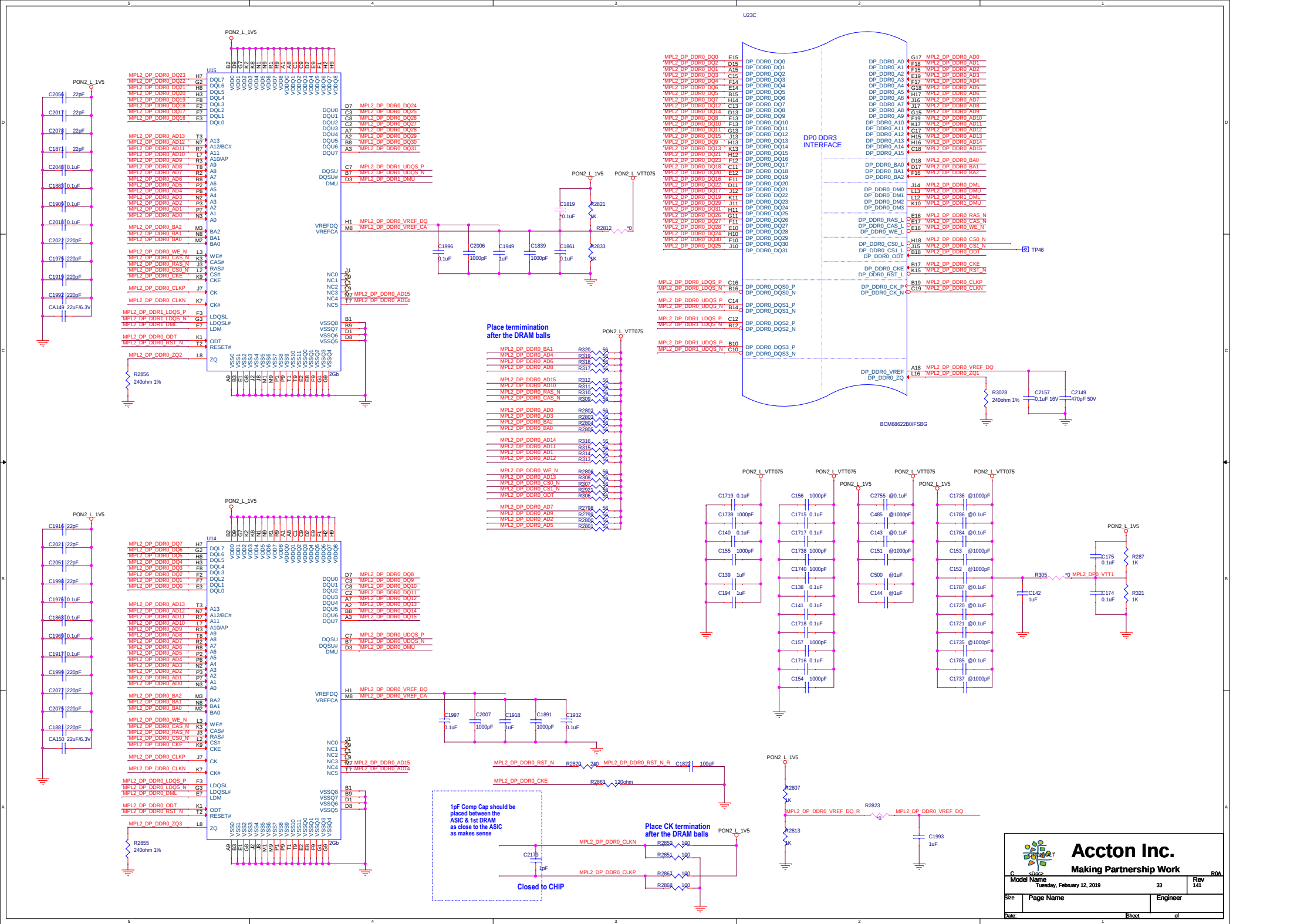


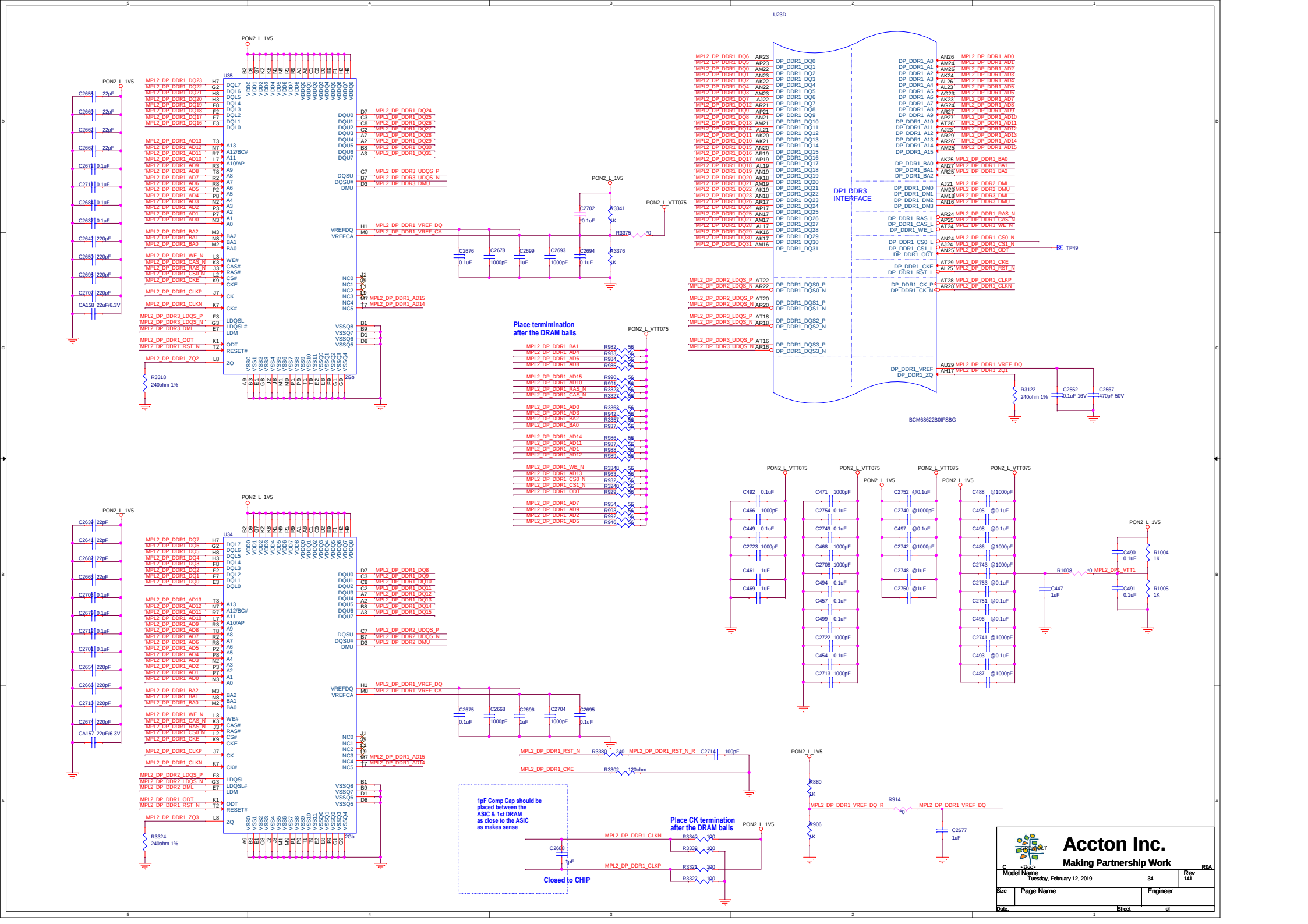
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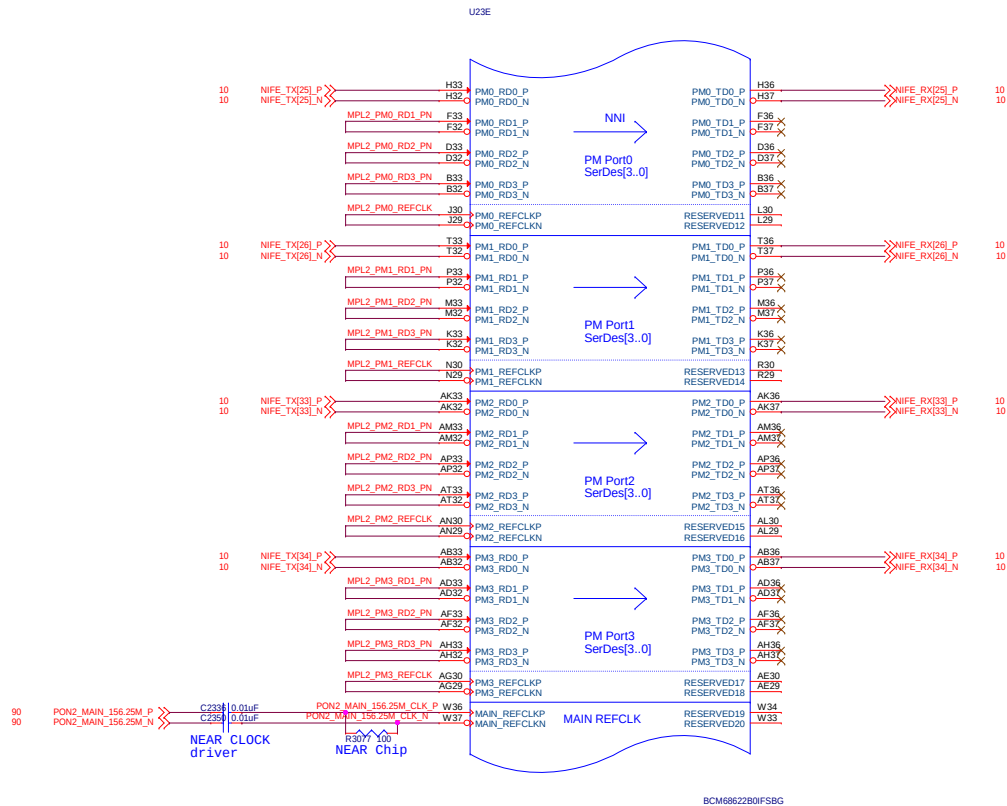


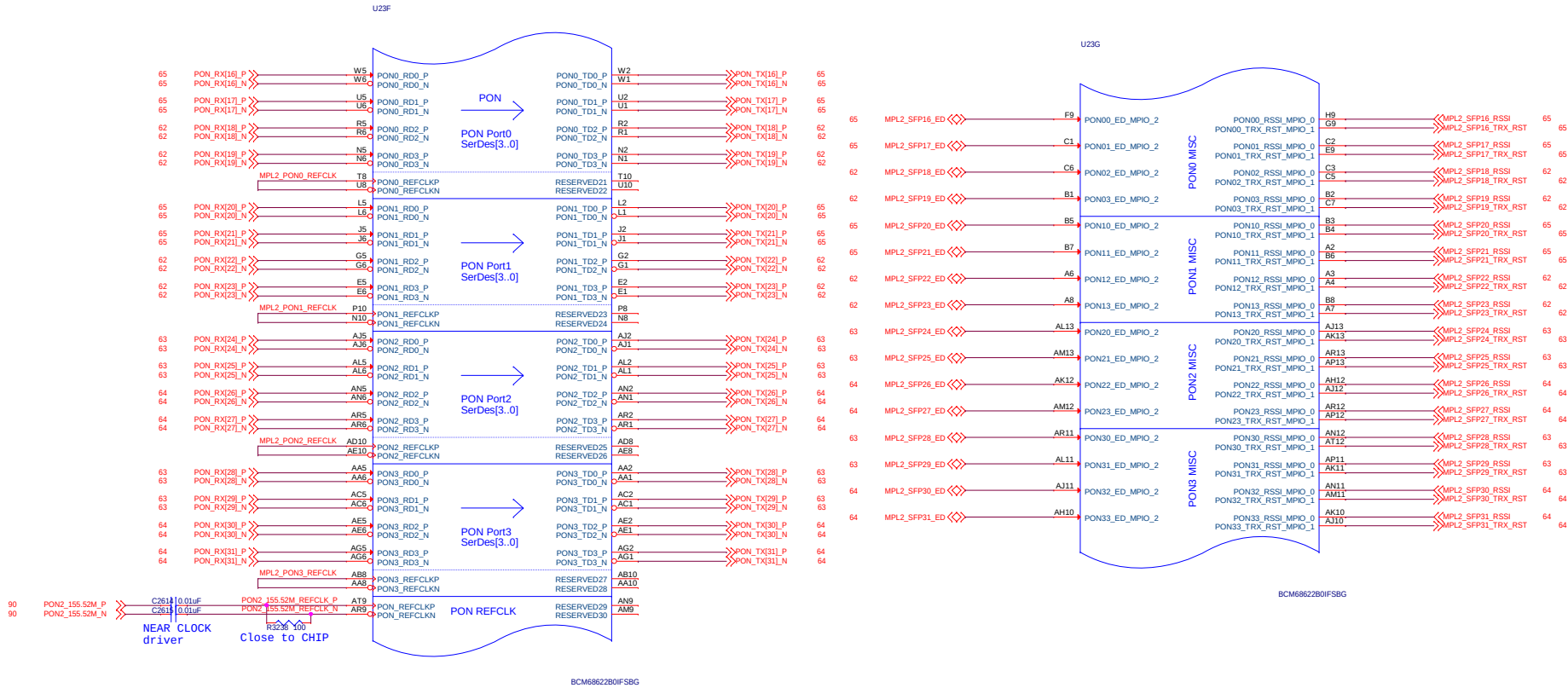
DDR3 Layout constrains

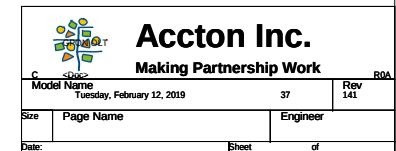
- The DDR_CLK_P/N signal from the ASIC should be routed in a fly-by from one SDRAM device to next
- The length of the clock trace the ASIC to DDR3-SDRAM device should be greater than or equal to the trace length of the DQS signal(s) from the ASIC to same SDRAM device
- The DQS, and DM signal are routed in a point-to-point fasion.
- 1.the length of every trace should be matched to within 30mils to other trace within the byte group.
- 2.To keep crosstalk to a minimum, keep trace separated from other trace by at least 3 times the trace wifth.(Typically 4 mil trace width *3 = 12 mil keep
- Address and control signal should be routed in a fly-by manner, like the DDR_CLK_P/N signal.
- 1.The length of every trace should be matched to within 150 mils to other trace within ADD/CTRL and DDR_CLK_P/N group.
- 2. Place termination to VTT after the last SDRAM balls.
- The trace width of VTT and VREF should be 40 mils minimum.
- Sometimes a PCB layout designer may want to swap data bits to simplify the routing of a data bus.
- For DDR3-SDRAM, it is permissible to swap data bits (though only within a byte lane).
- Keep the maximum byte-lane group-to-byte group matched length deviation to +- 0.2 inched.

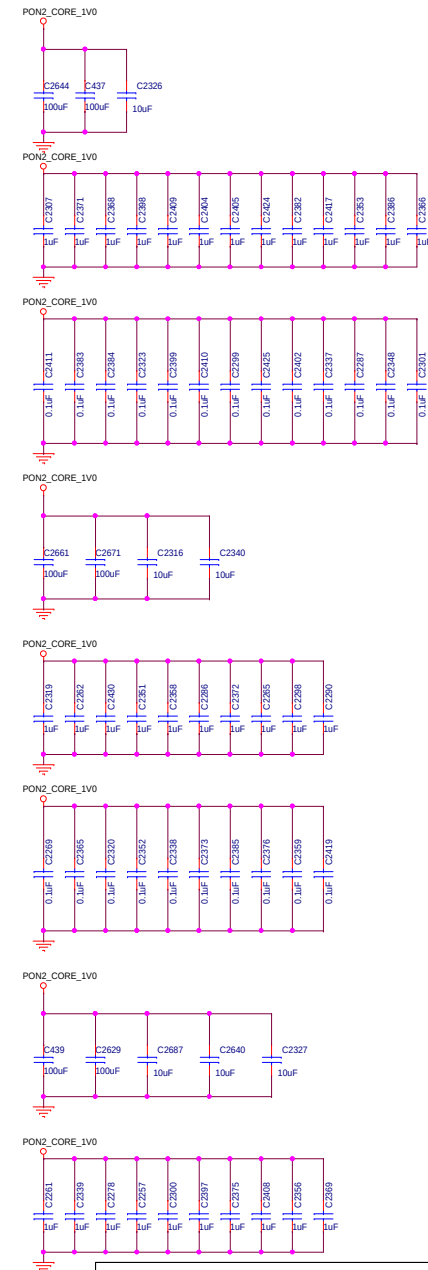


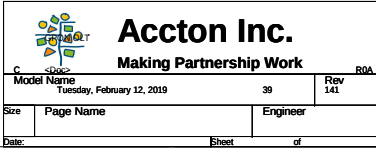


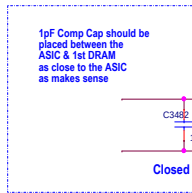




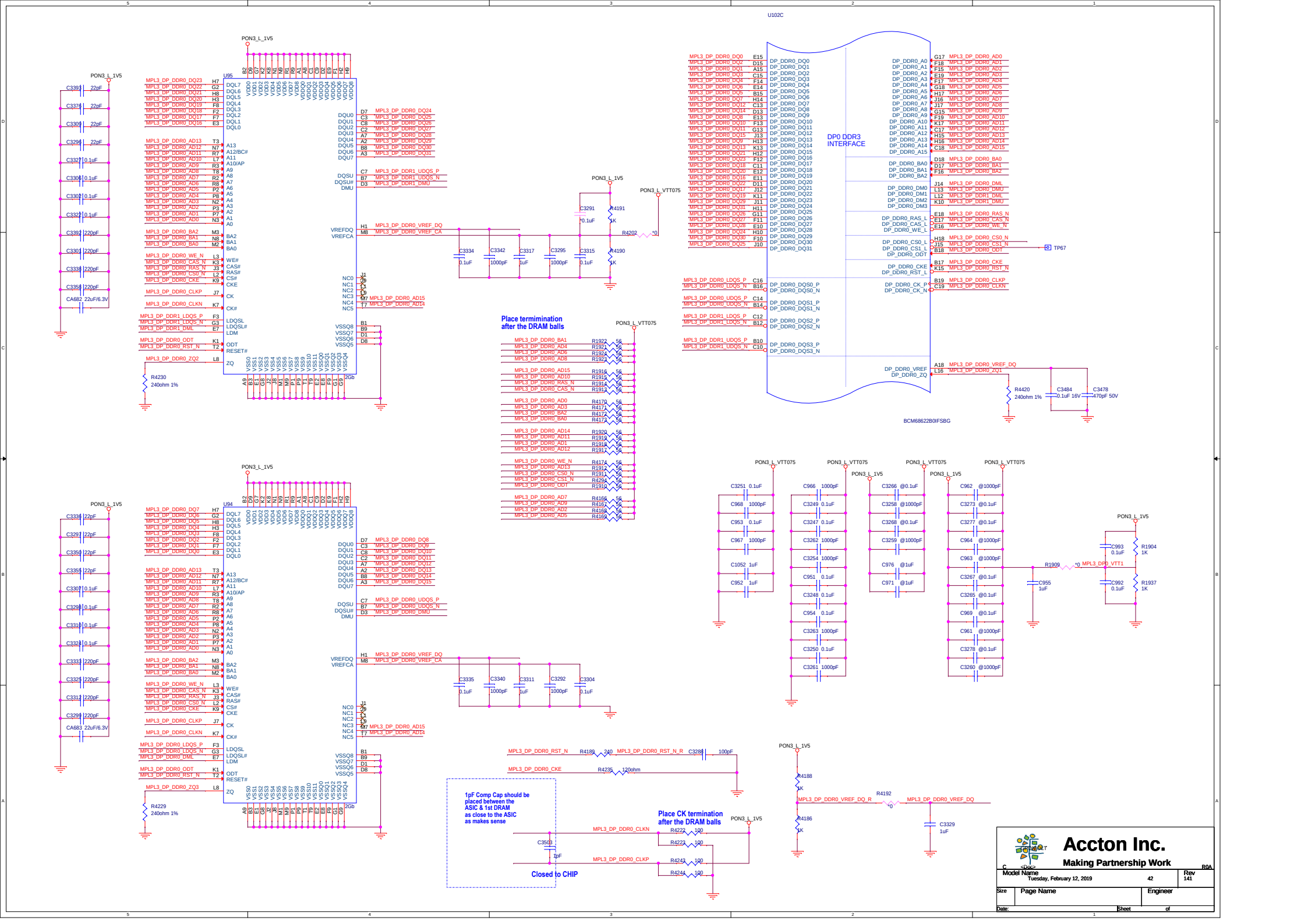


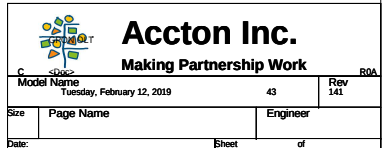


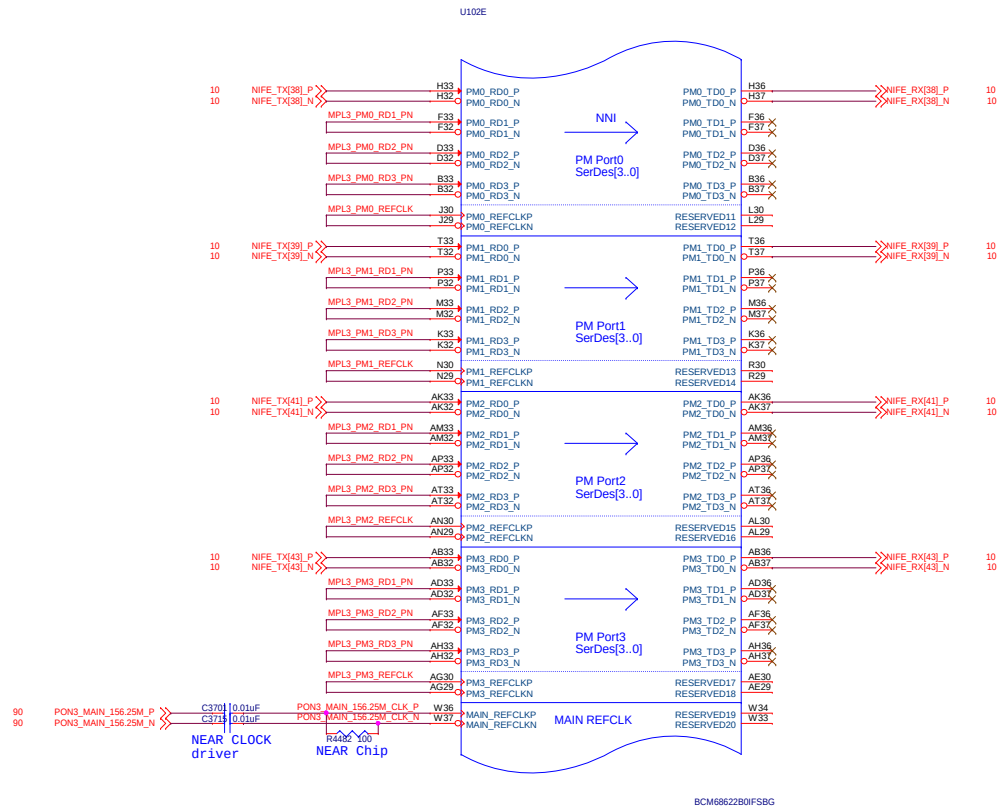


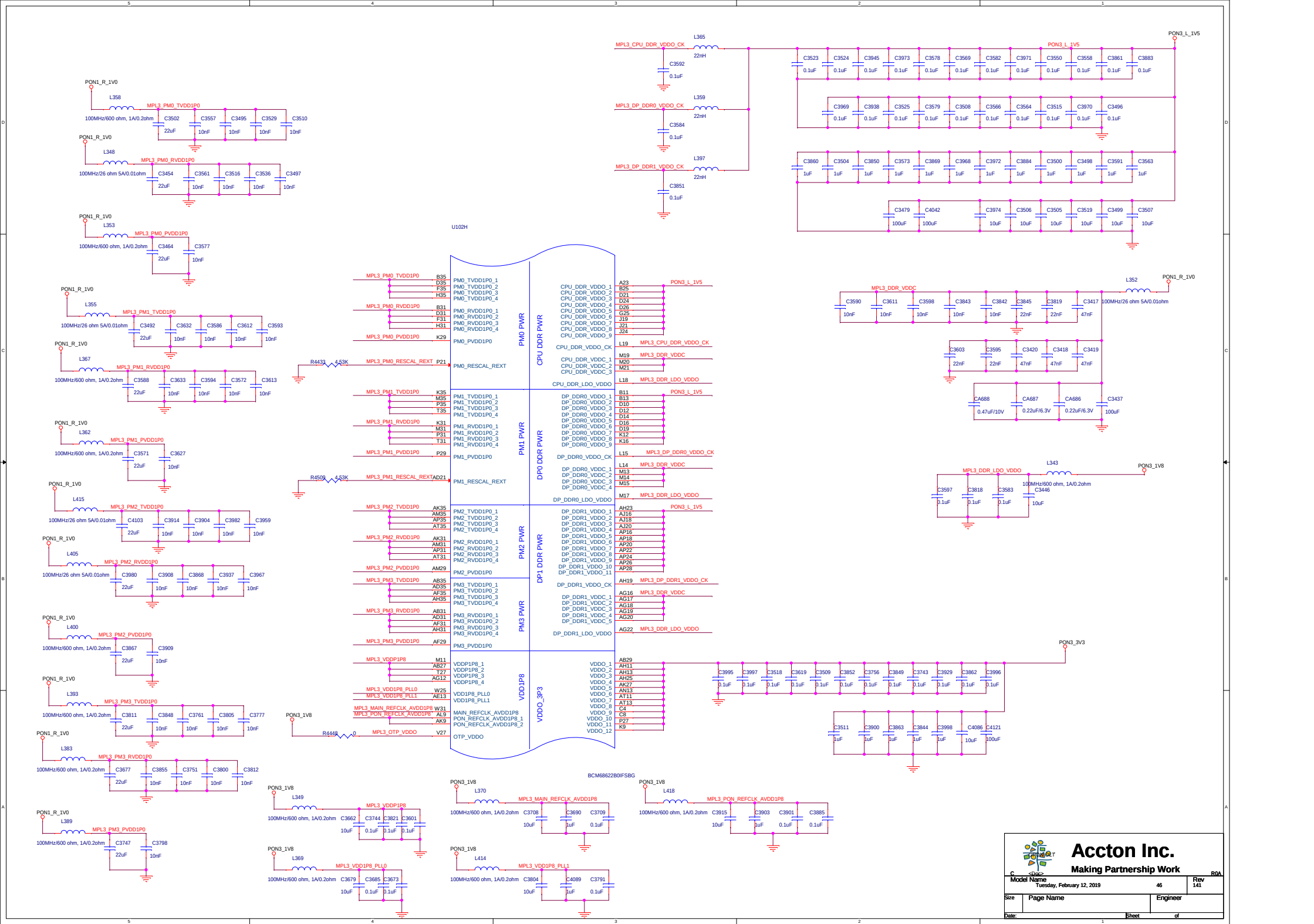


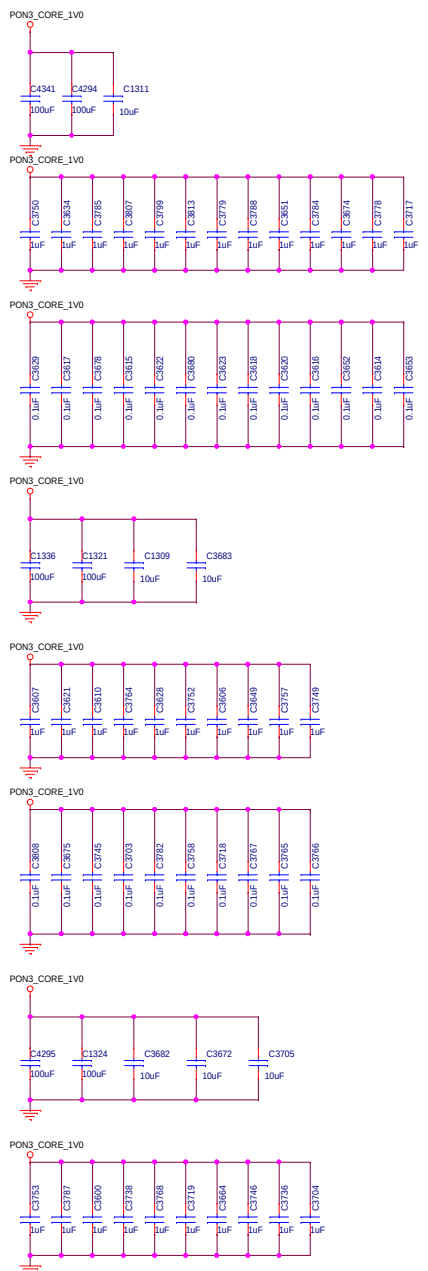
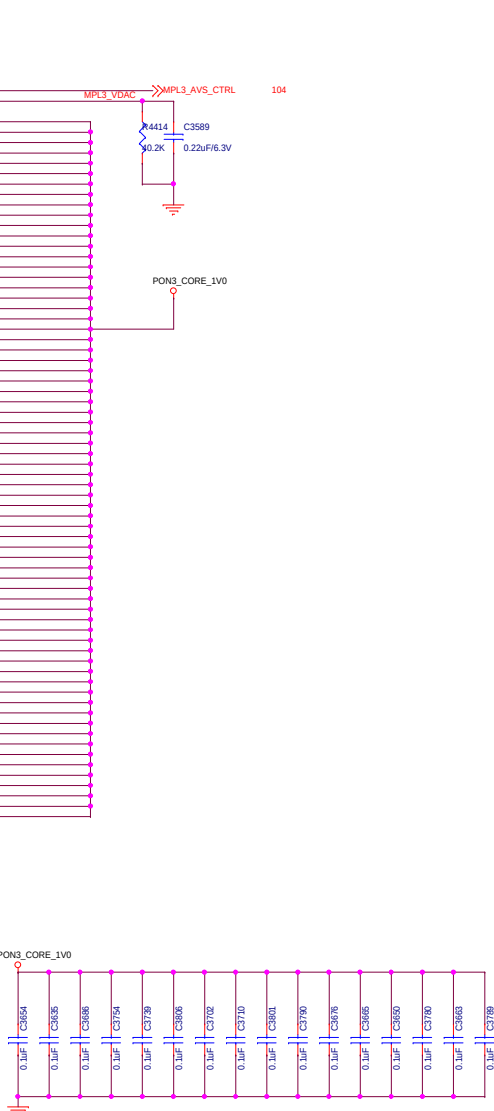
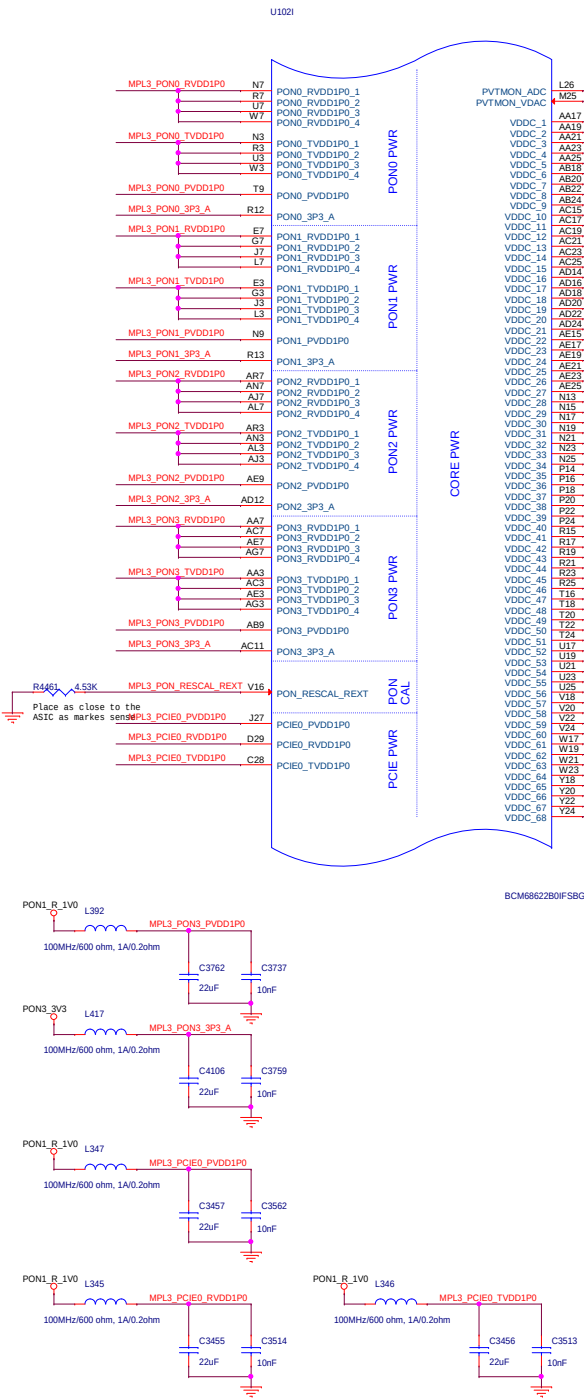
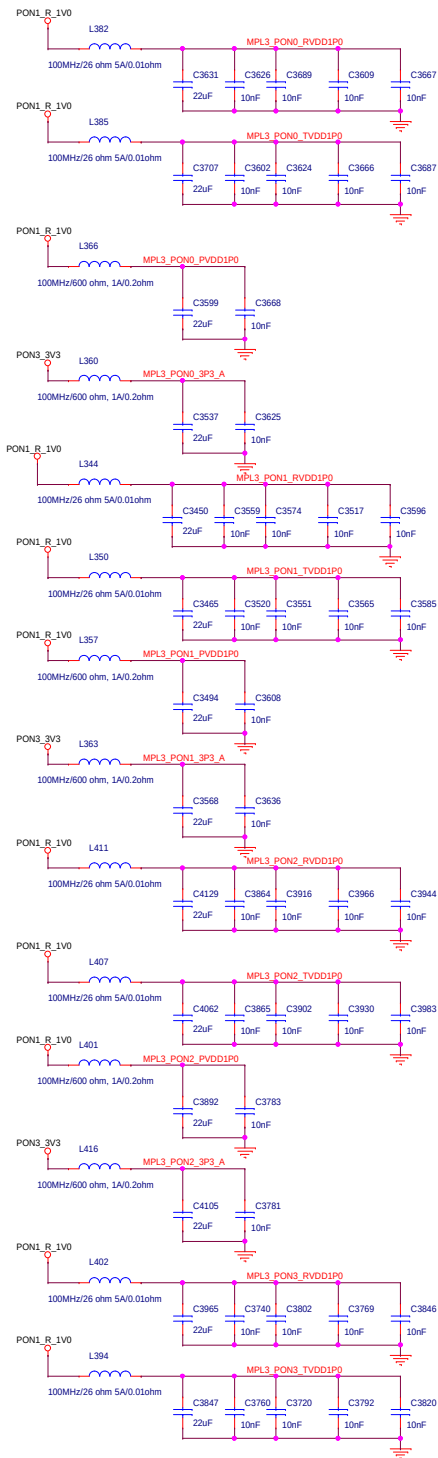
The DDR_CLK_P/N signal from the ASIC should be routed in a fly-by from one SDRAM device to next.
 The length of the clock trace the ASIC to DDR3-SDRAM device should be greater than or equal to the trace length of the DQS signal(s) from the ASIC to same SDRAM device.
 The DQS, and DM signal are routed in a point-to-point fashion.
 1. The length of every trace should be matched to within 30mils to other trace within the byte group.
 2. To keep crosstalk to a minimum, keep trace separated from other trace by at least 3 times the trace width. (Typically 4 mil trace width * 3 = 12 mil keep off)
 Address and control signal should be routed in a fly-by manner, like the DDR_CLK_P/N signal.
 1. The length of every trace should be matched to within 150 mils to other trace within ADD/CTRL and DDR_CLK_P/N group.
 2. Place termination to VTT after the last SDRAM balls.
 The trace width of VTT and VREF should be 40 mils minimum.
 Sometimes a PCB layout designer may want to swap data bits to simplify the routing of a data bus.
 For DDR3-SDRAM, it is permissible to swap data bits (though only within a byte lane).
 Keep the maximum byte-lane group-to-byte group matched length deviation to +/- 0.2 inches.



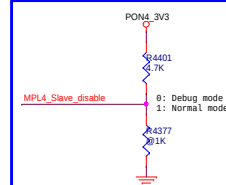






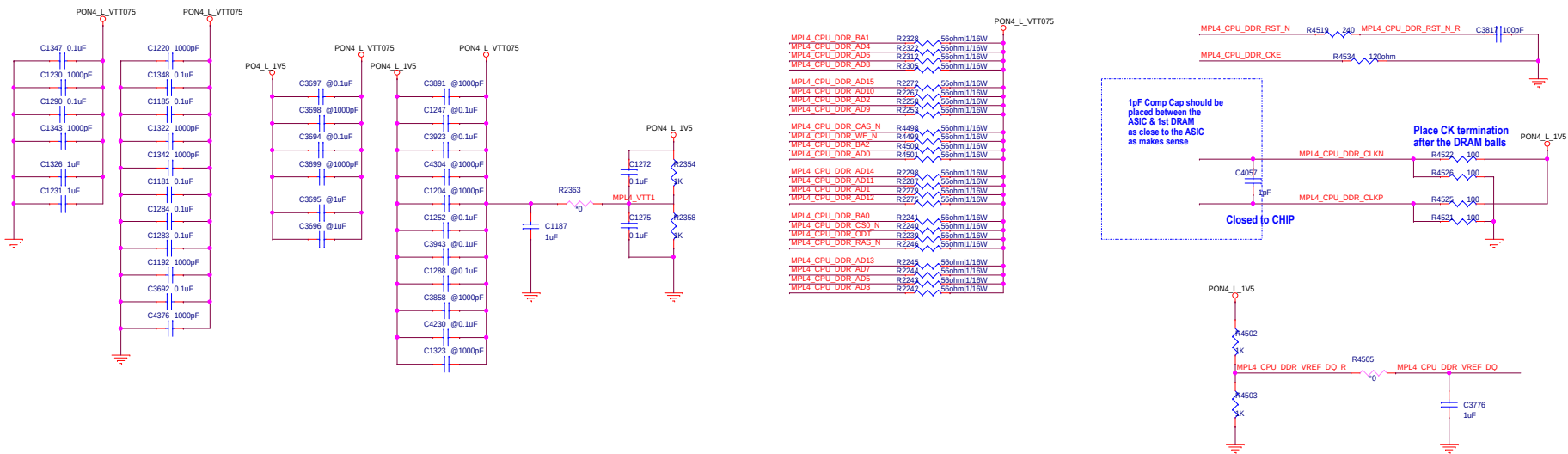
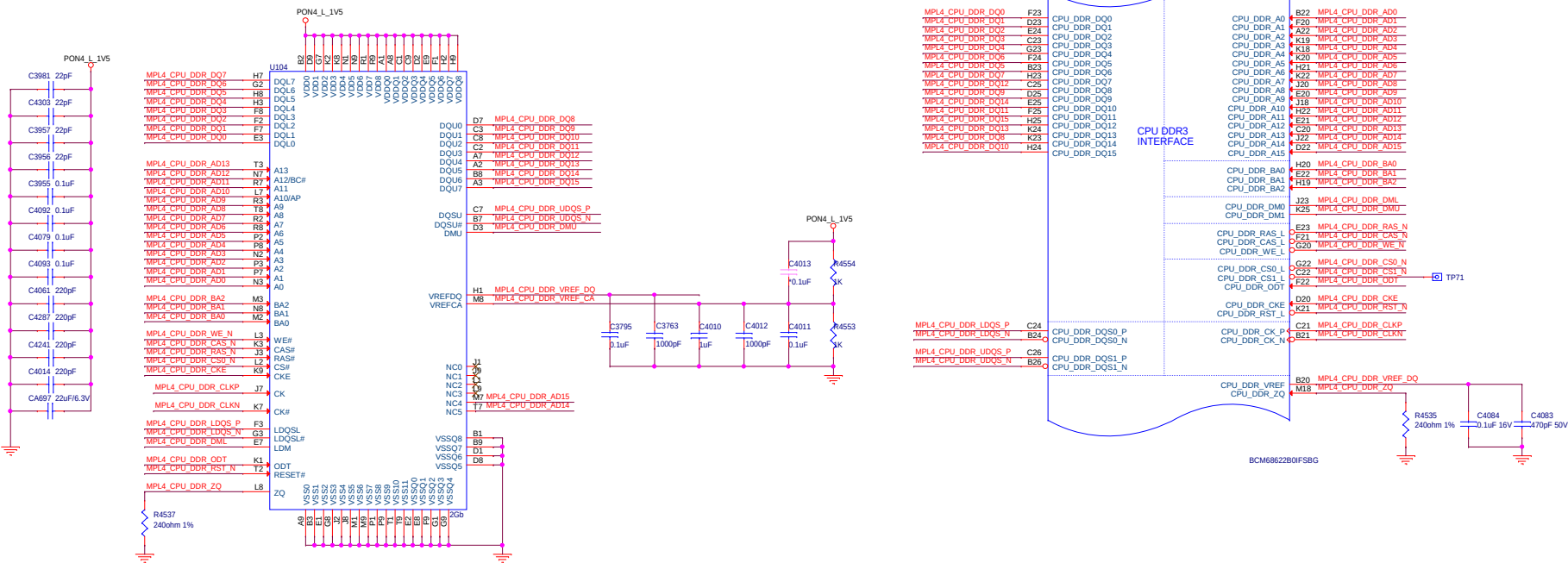






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DDR3 Layout constraints

The DDR_CLK_P/N signal from the ASIC should be routed in a fly-by from one SDRAM device to next

The length of the clock trace the ASIC to DDR3-SDRAM device should be greater than or equal to the trace length of the DQS signal(s) from the ASIC to same SDRAM device

.The DQS, and DM signal are routed in a point-to-point fasion.

1.the length of every trace should be matched to within 30mils to other trace within the byte group.

- 1.The length of every trace should be matched to within 50 mils to other trace within the byte group.
- 2.To keep crosstalk to a minimum, keep trace separated from other trace by at least 3 times the trace width. (Typically 4 mil trace width *3 = 12 mil keep out zone)

.Address and control signal should be routed in a fly-by manner , like the DDR CLK P/N signal.

1. The length of every trace should be matched to within

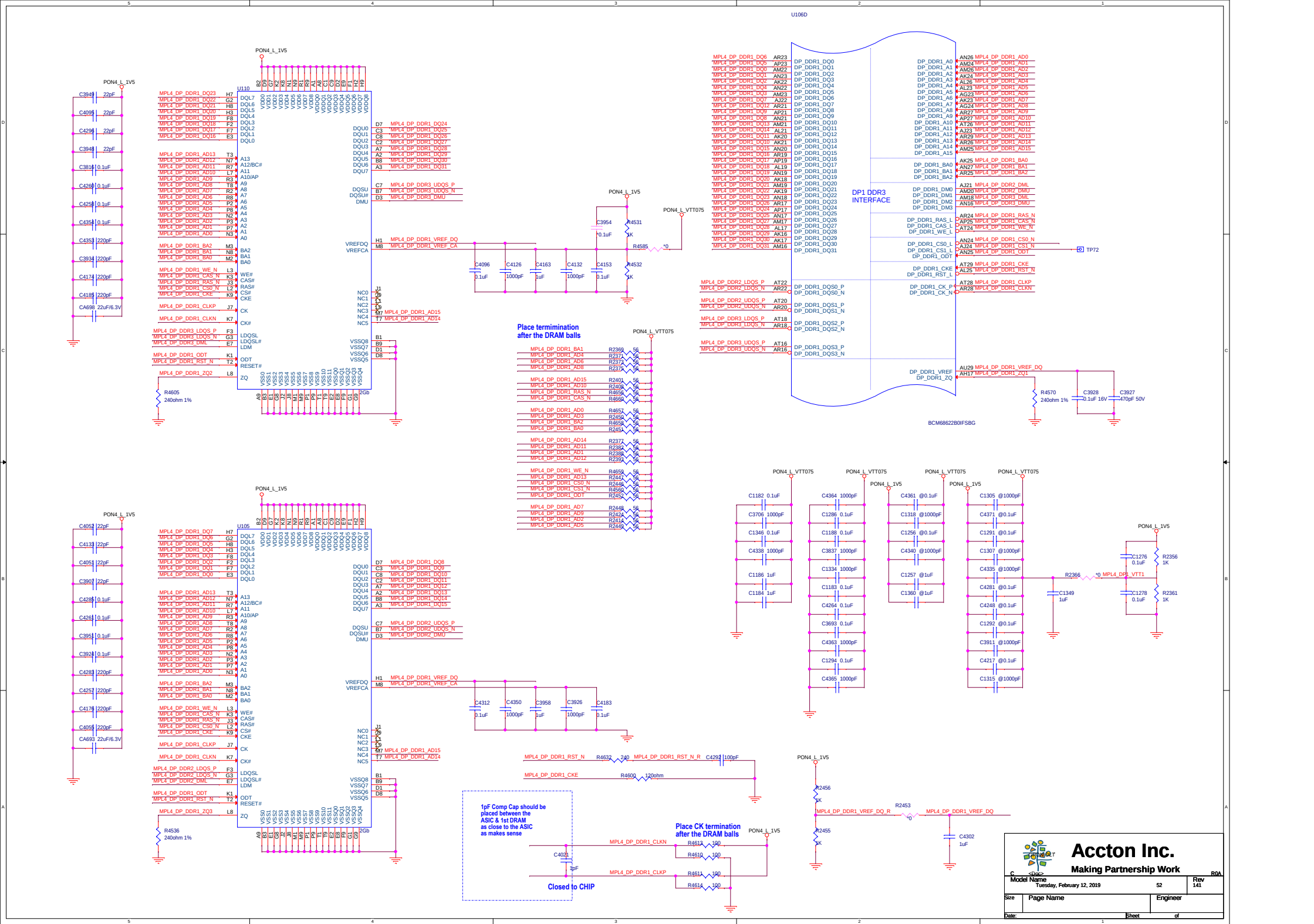
1. The length of every trace should be matched to within 1
2. Place termination to VTT after the last SDRAM balls.

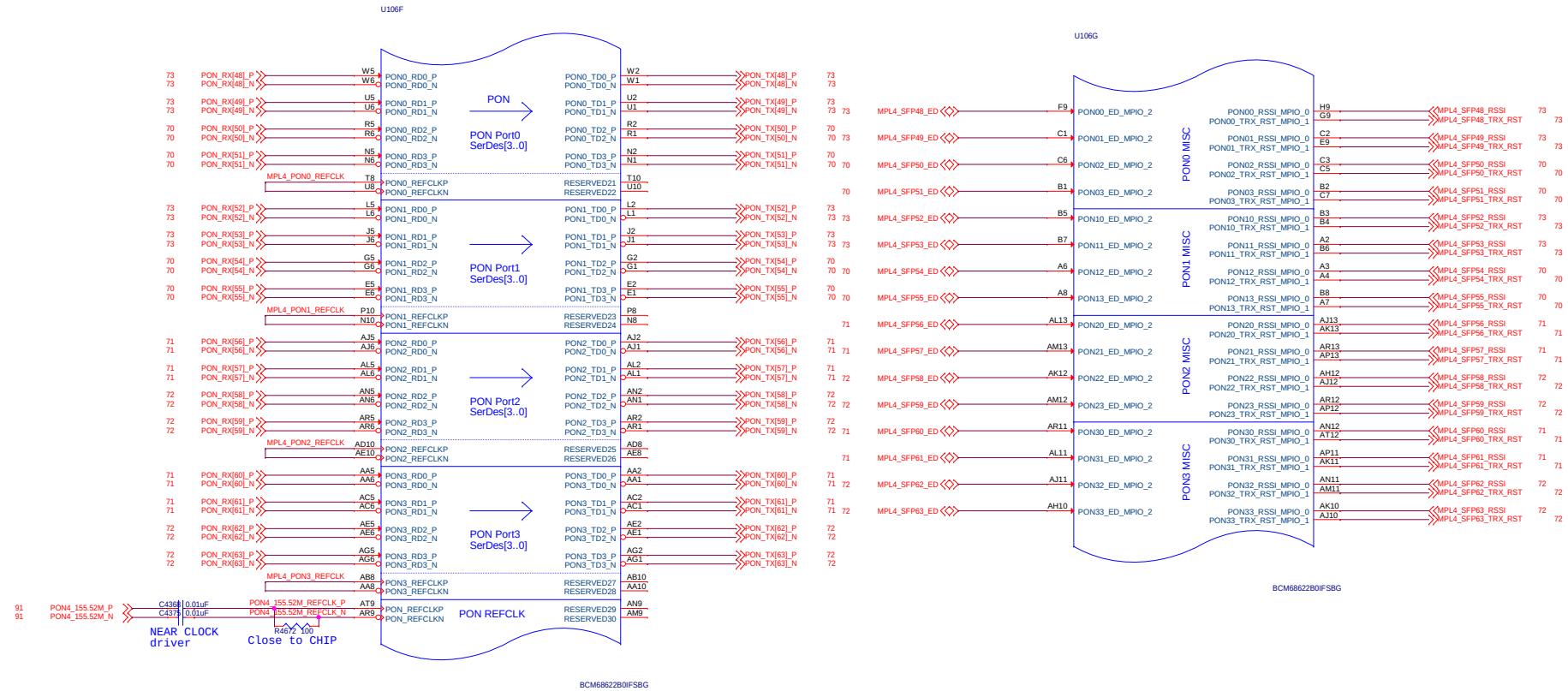
.The trace width of VTT and VREF should be 40 mils minimum.

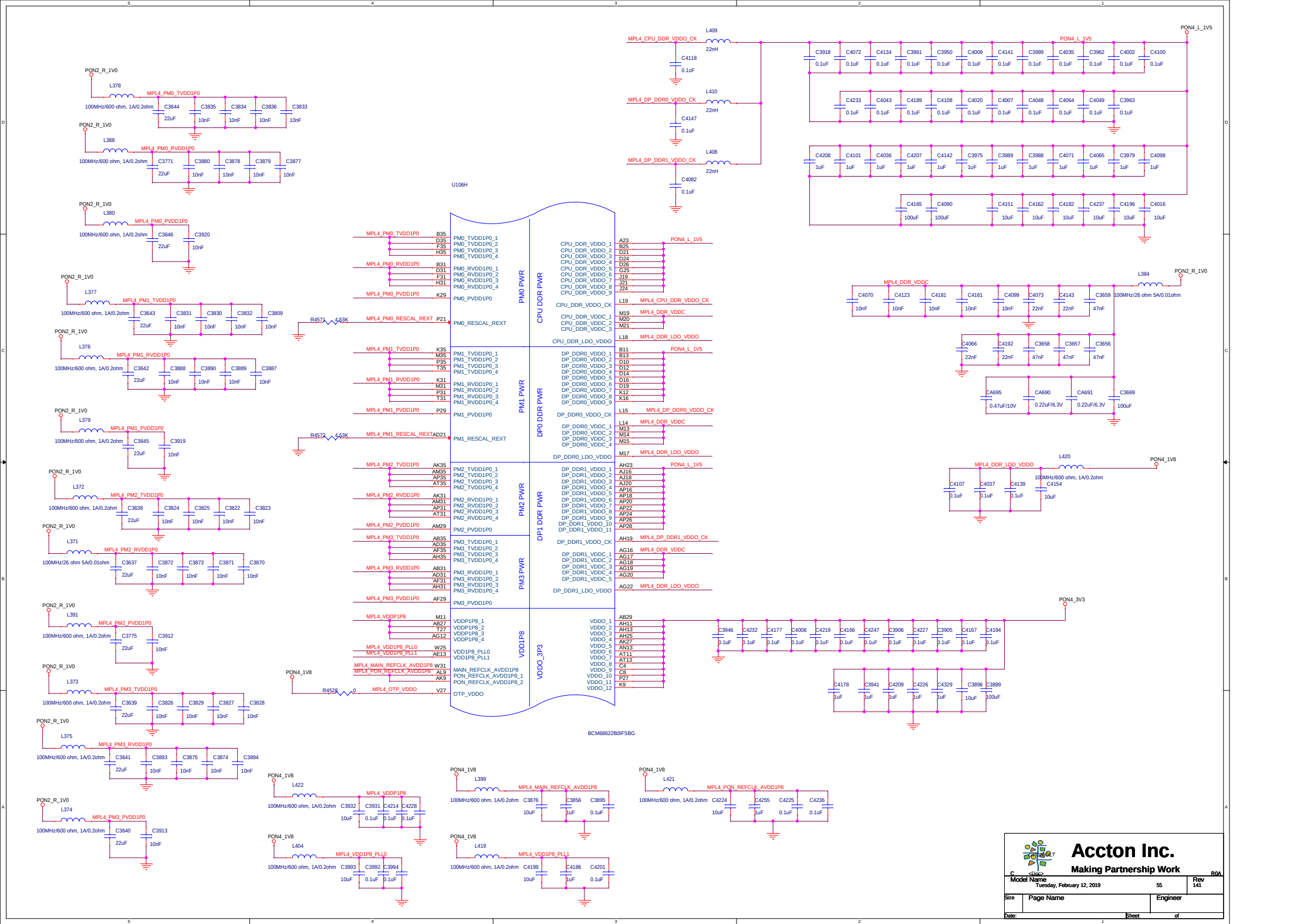
• Sometimes a PCB layout designer may want to swap data bits to simplify the routing of a data bus.

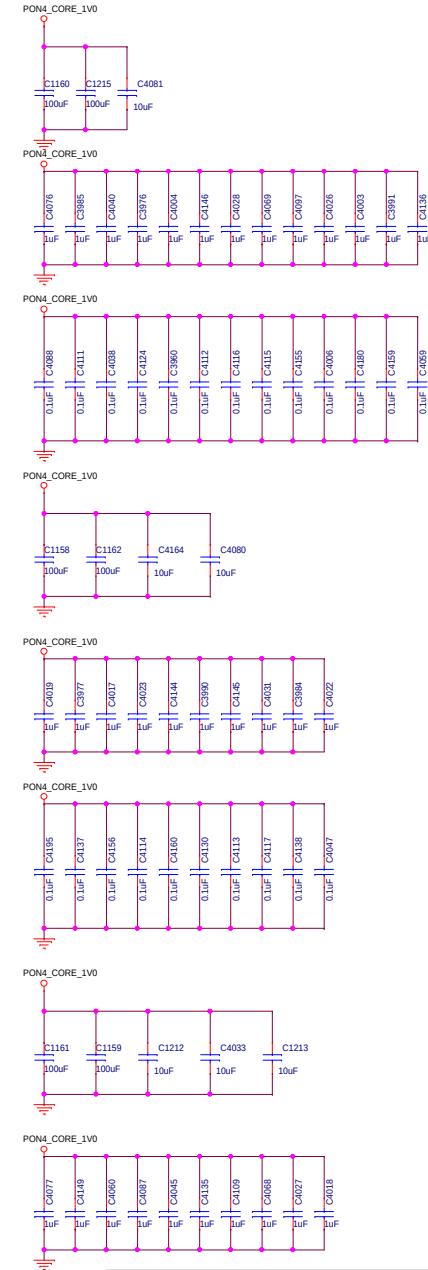
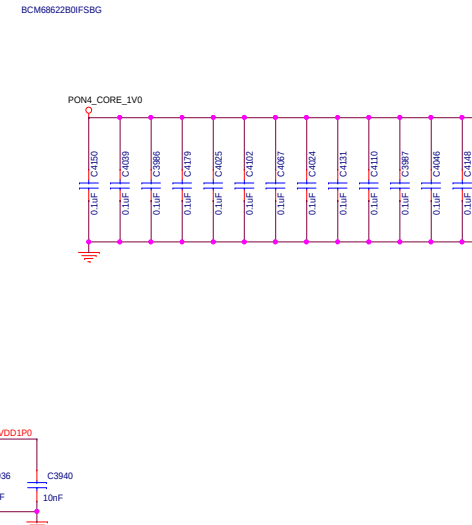
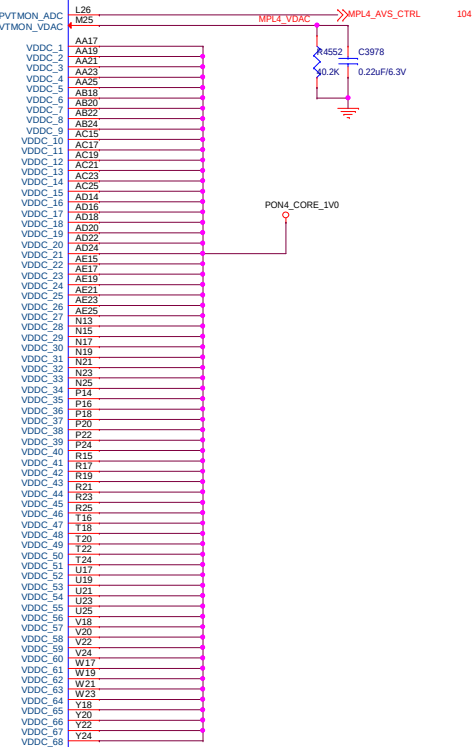
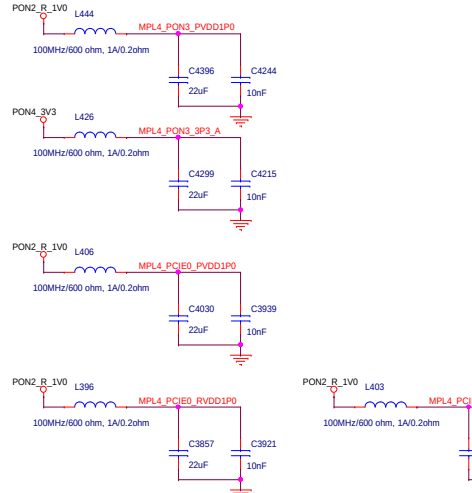
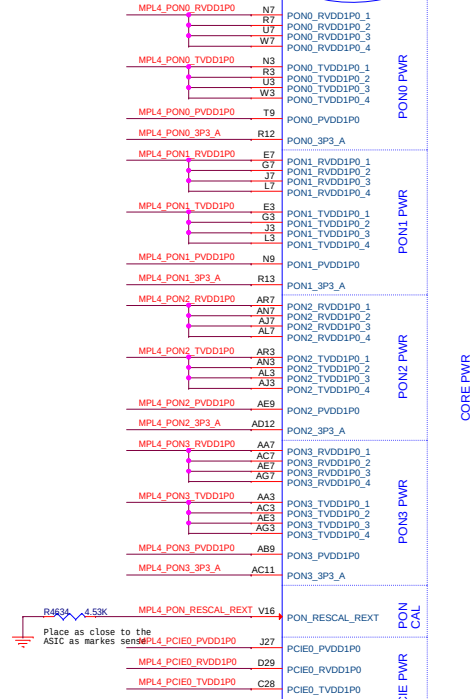
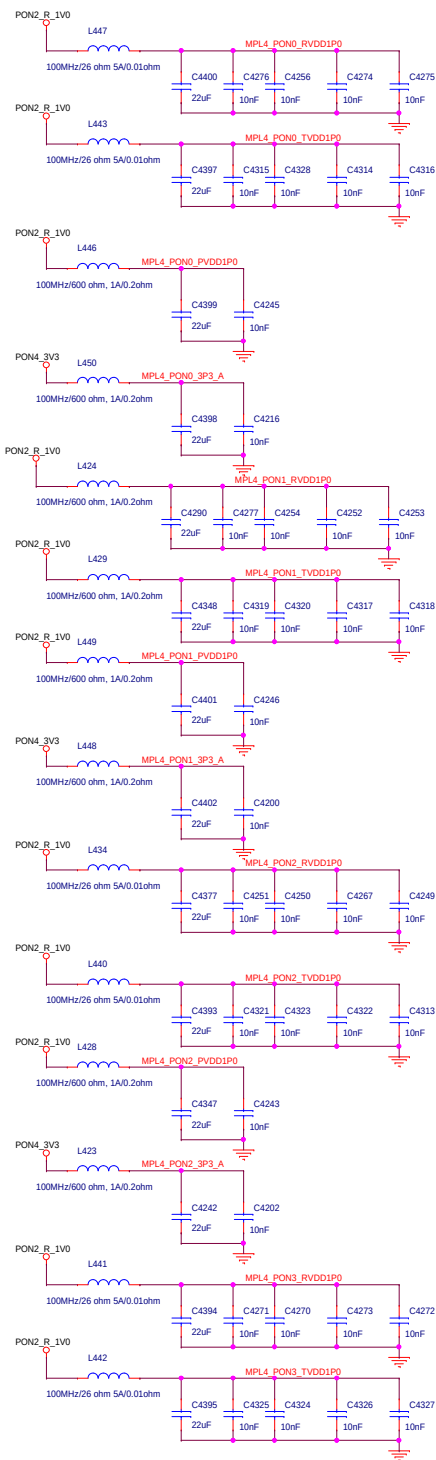
For DDR3-SDRAM, it is permissible to swap data bits (though only within a byte lane).

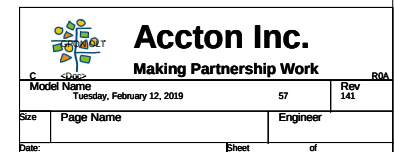
Keep the maximum byte-lane group-to-byte group matched length deviation to ± 0.2 inches.

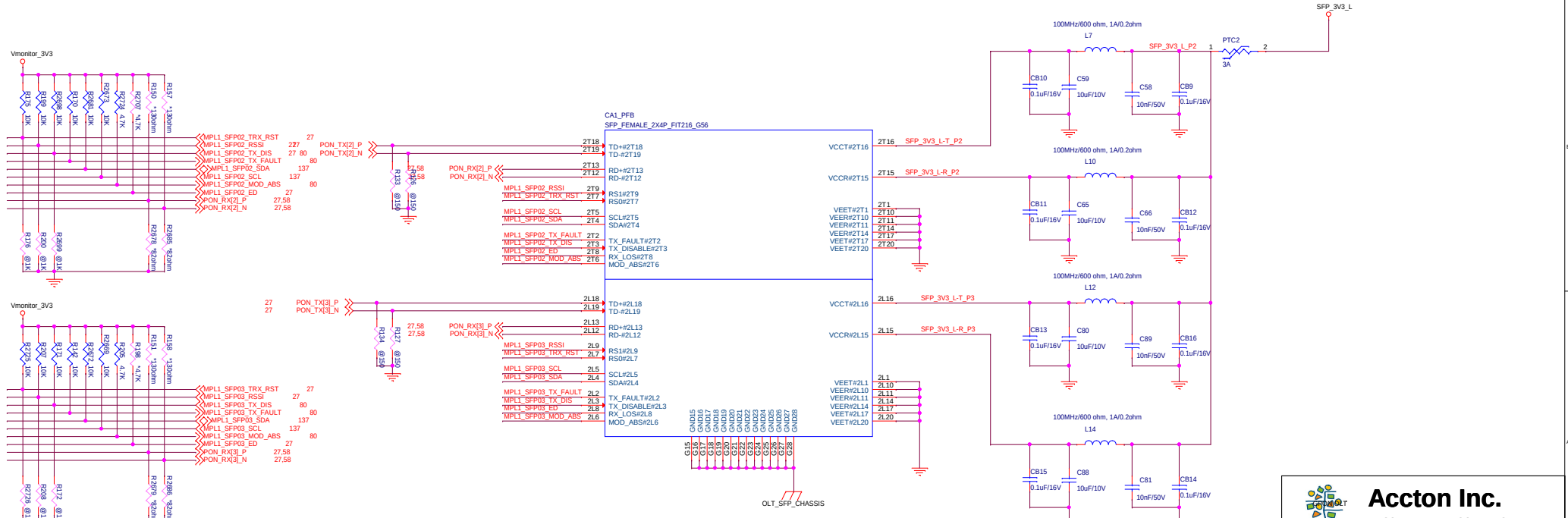
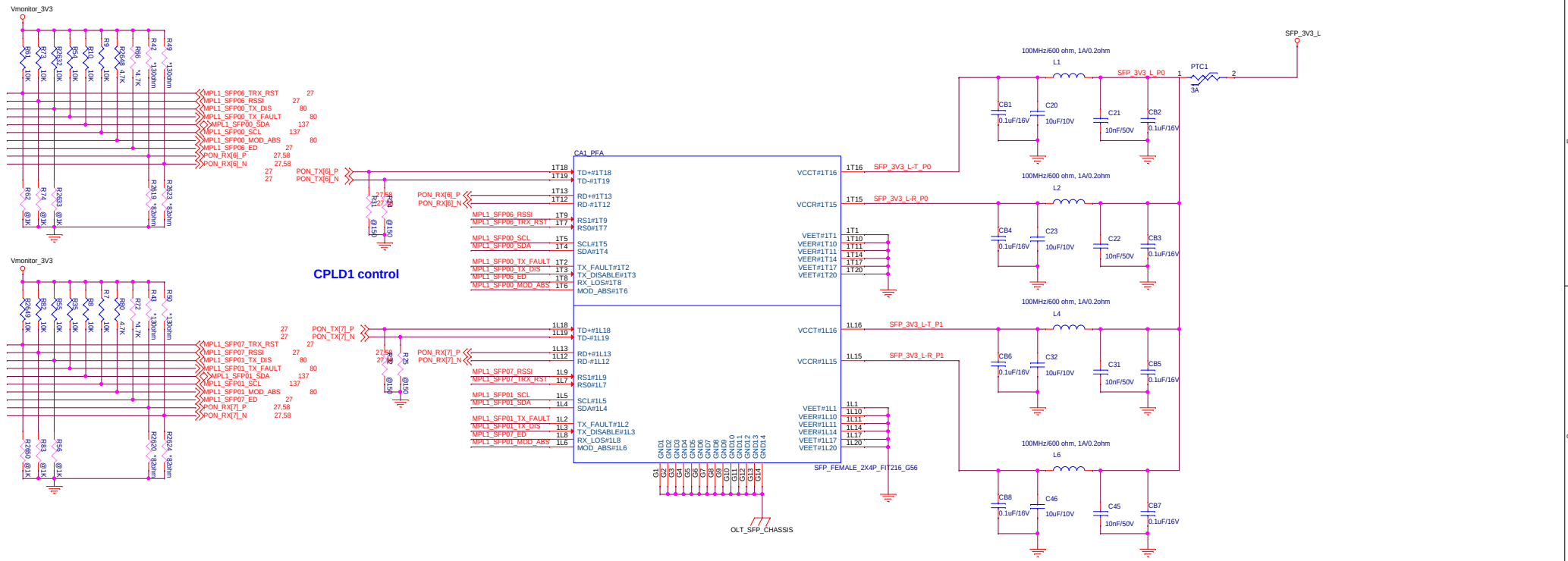


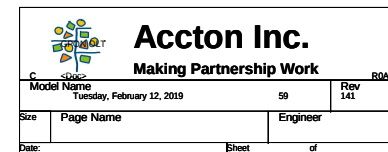


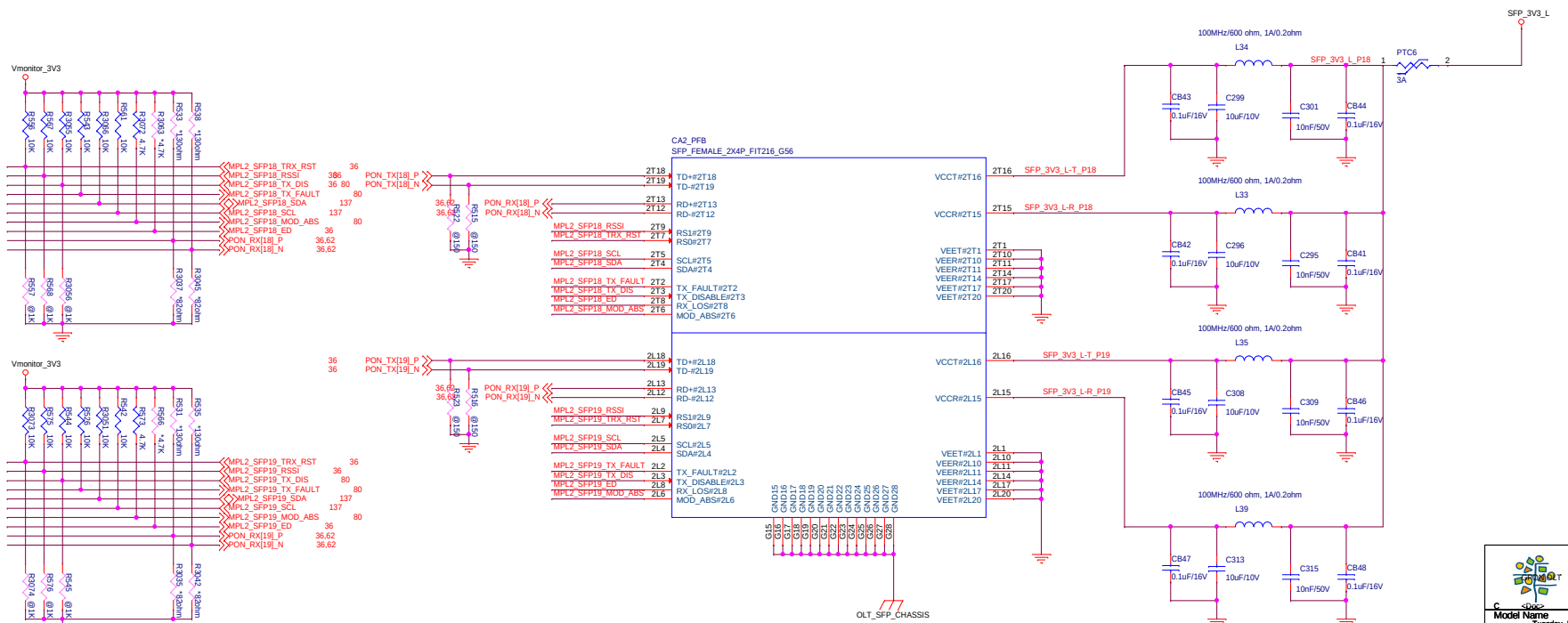


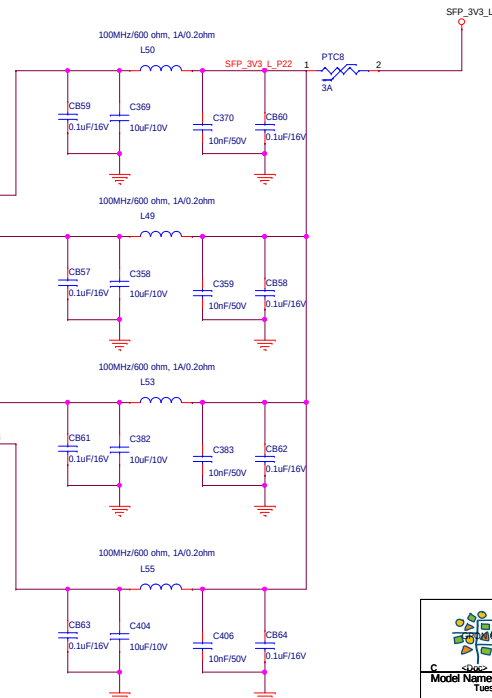
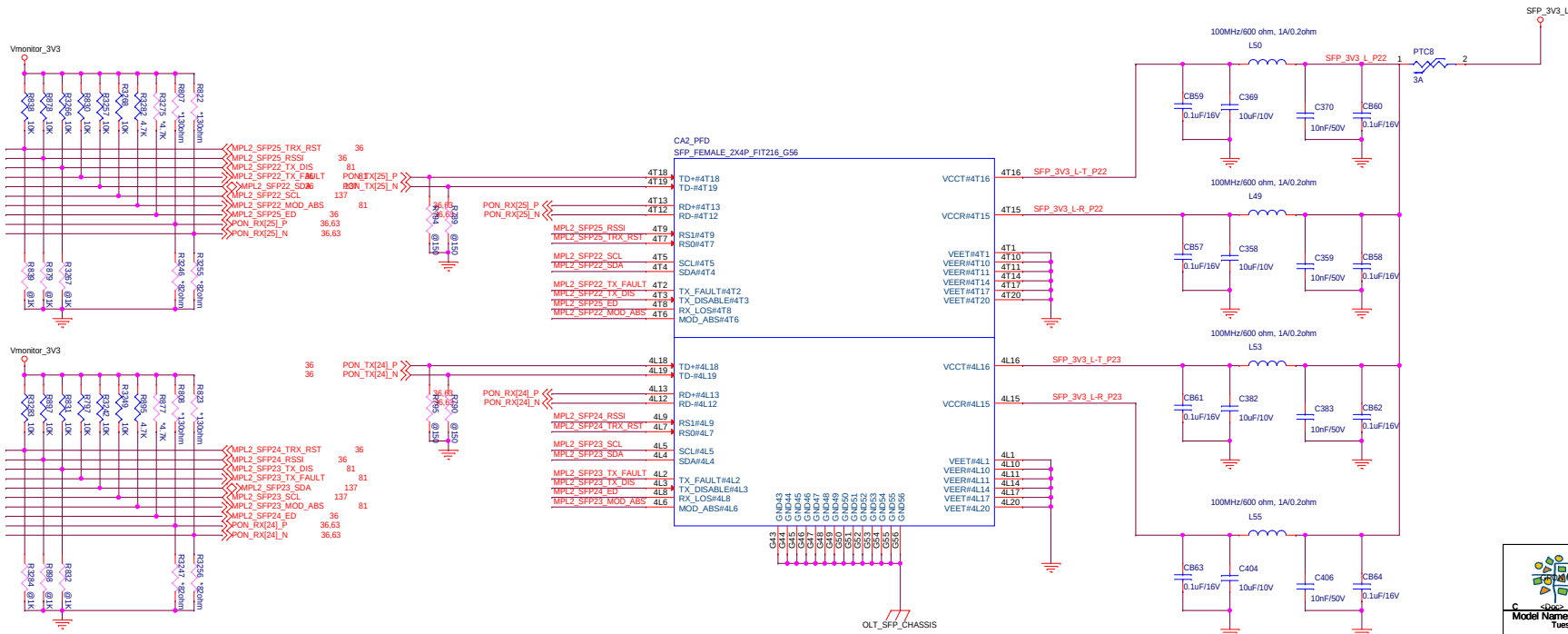


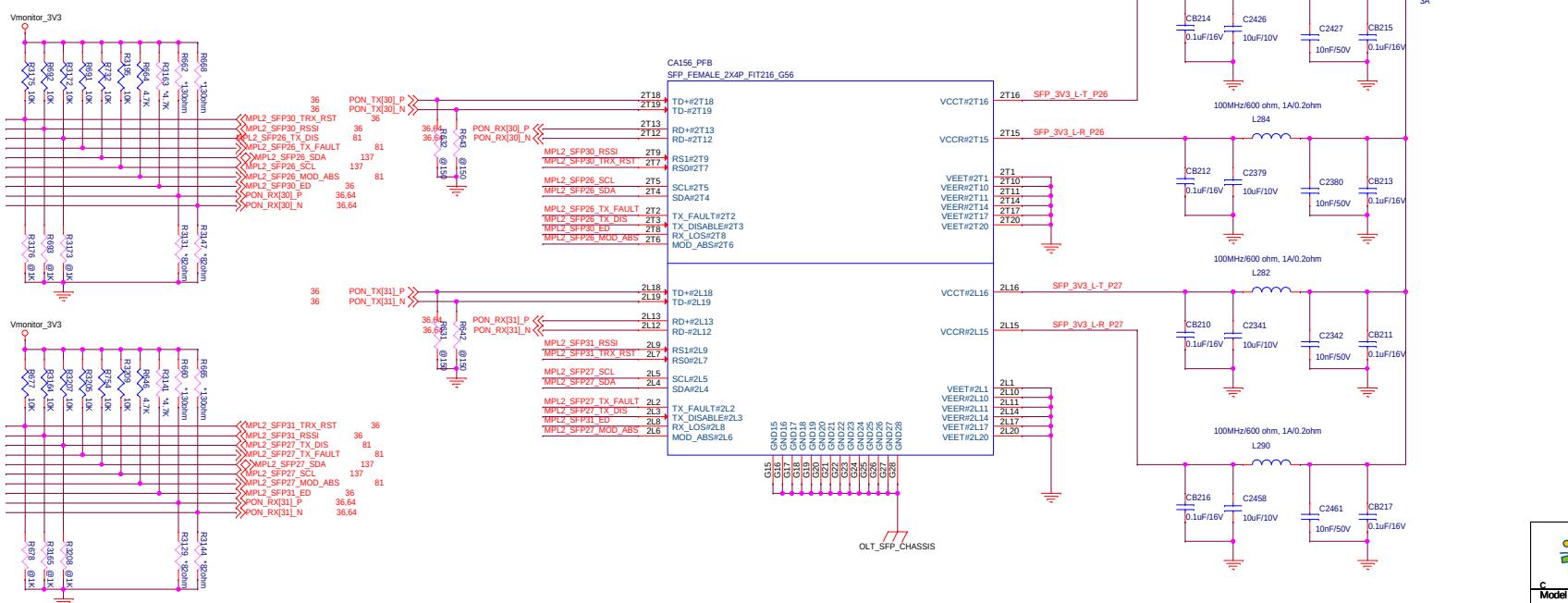
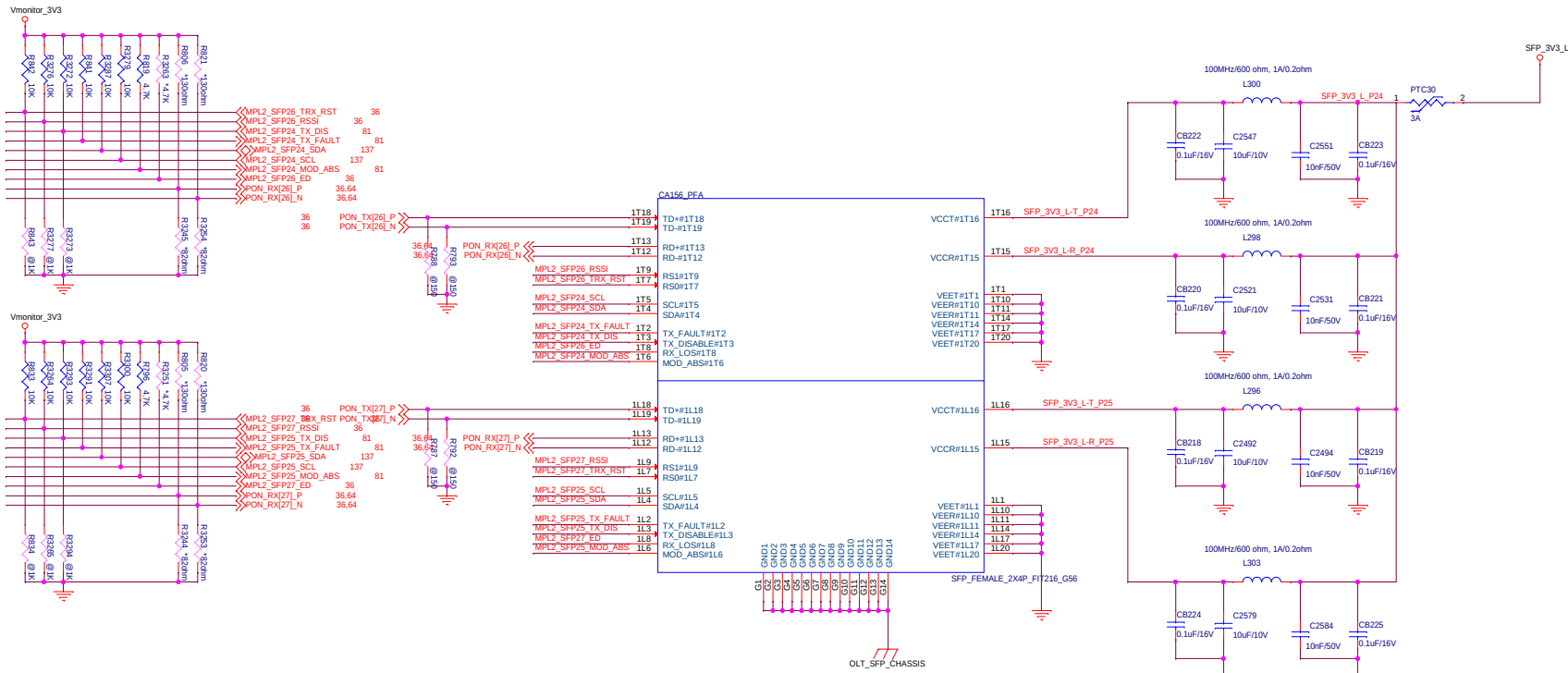


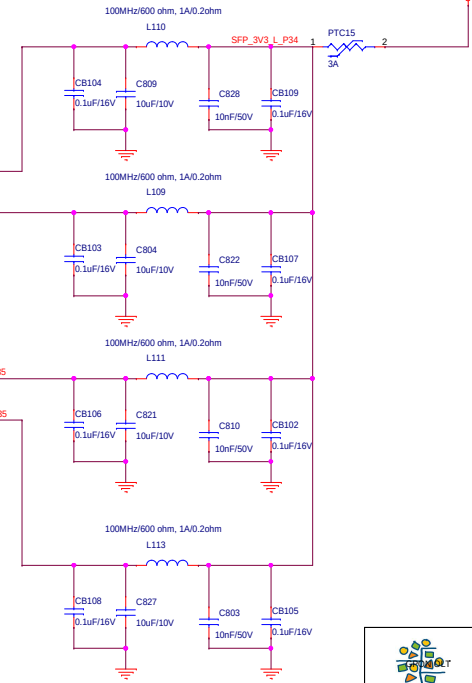
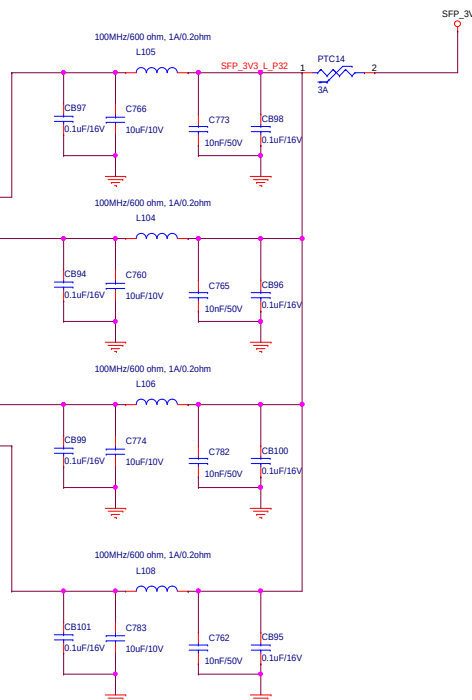


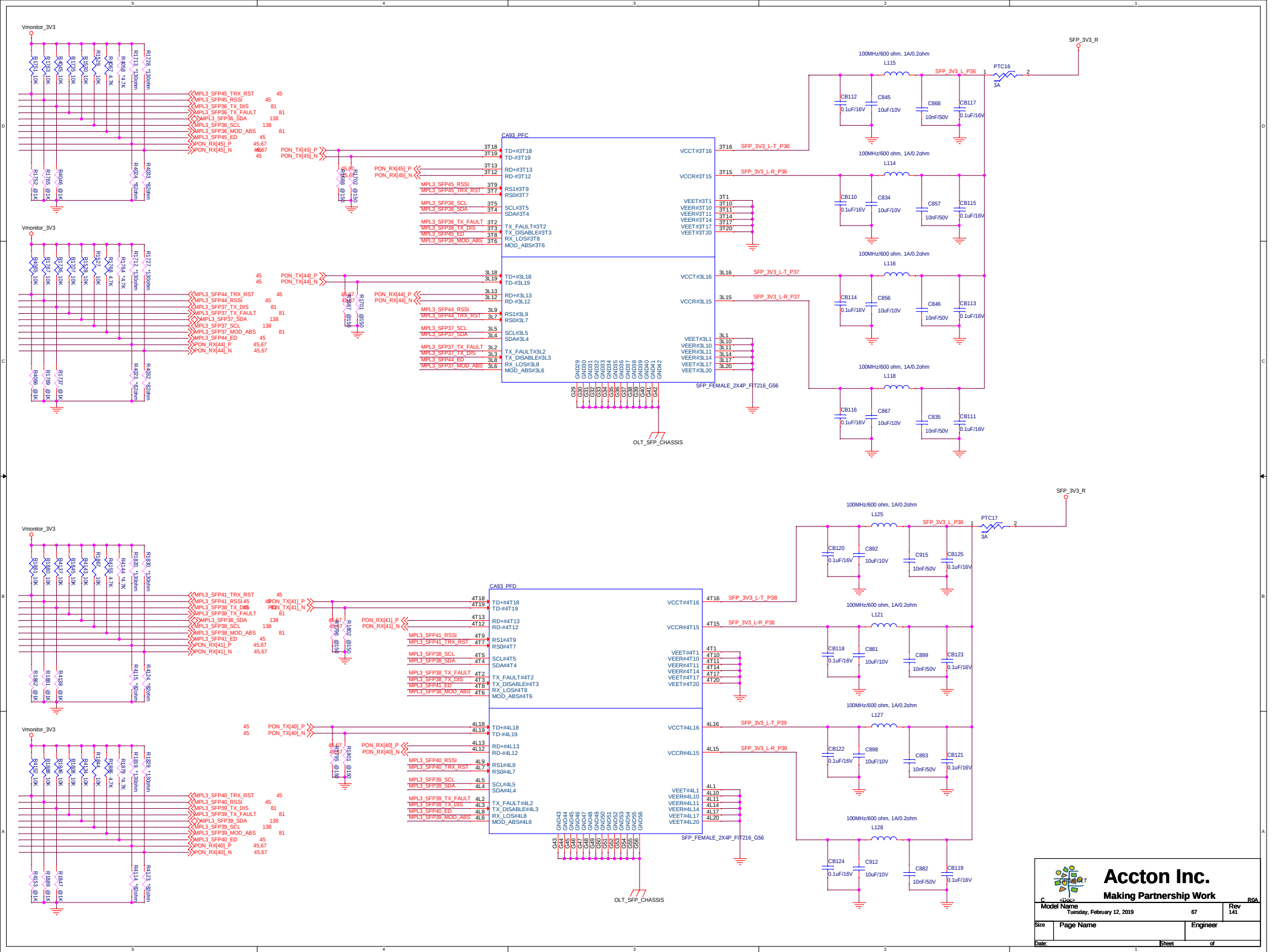


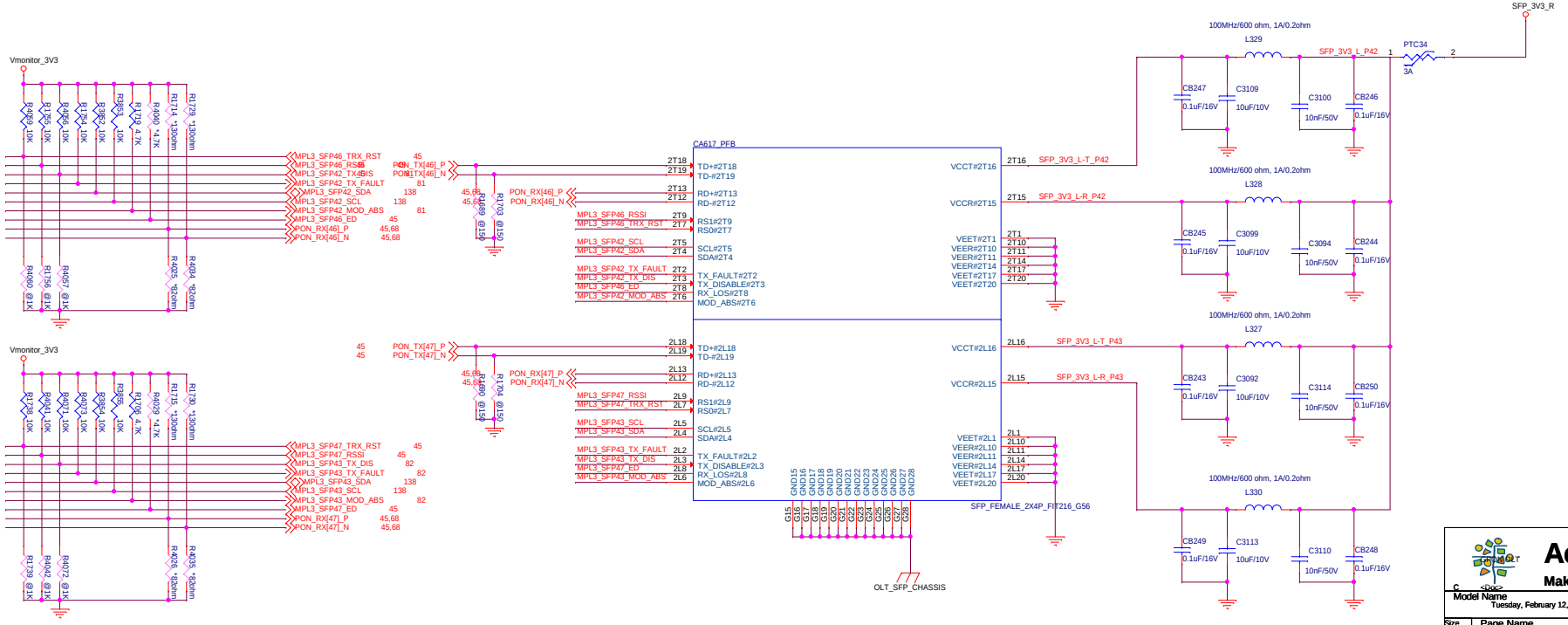
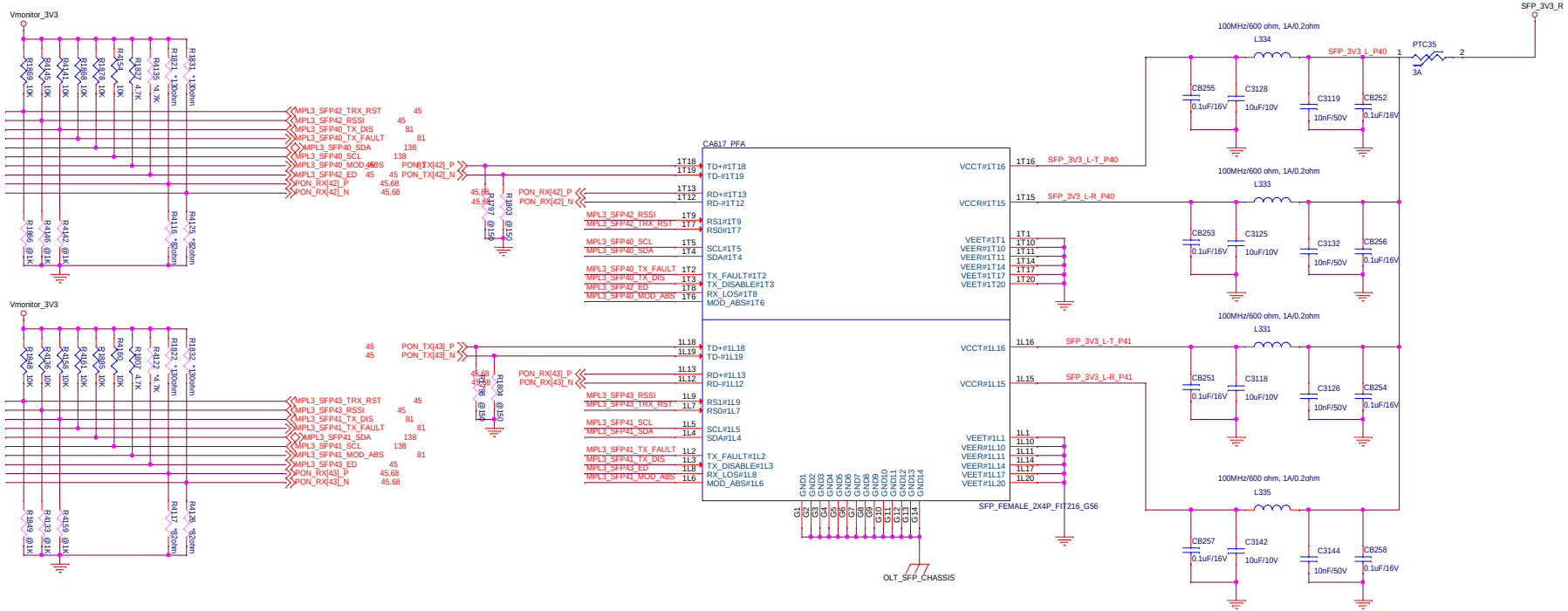


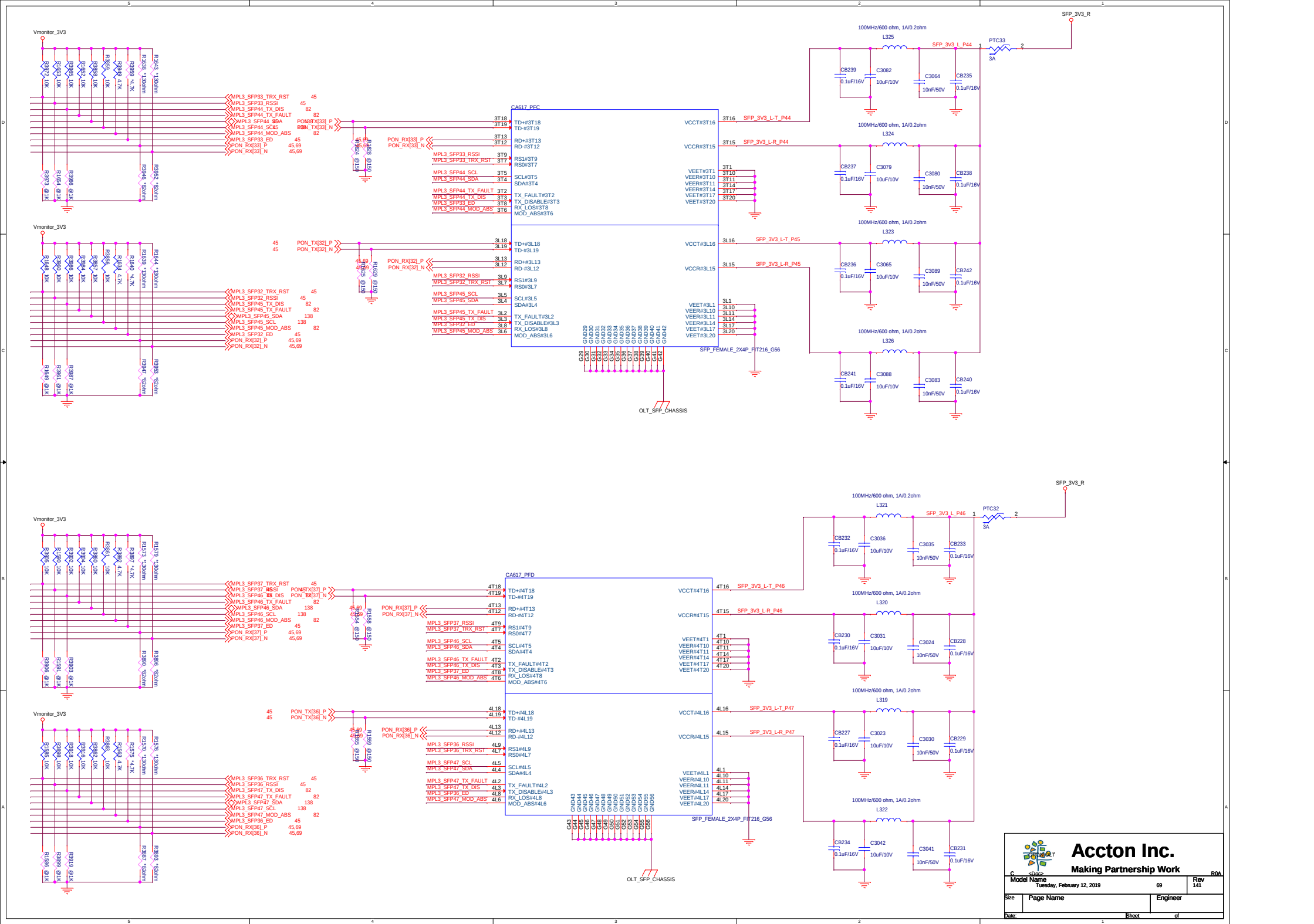


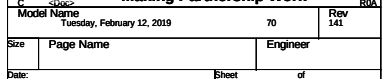
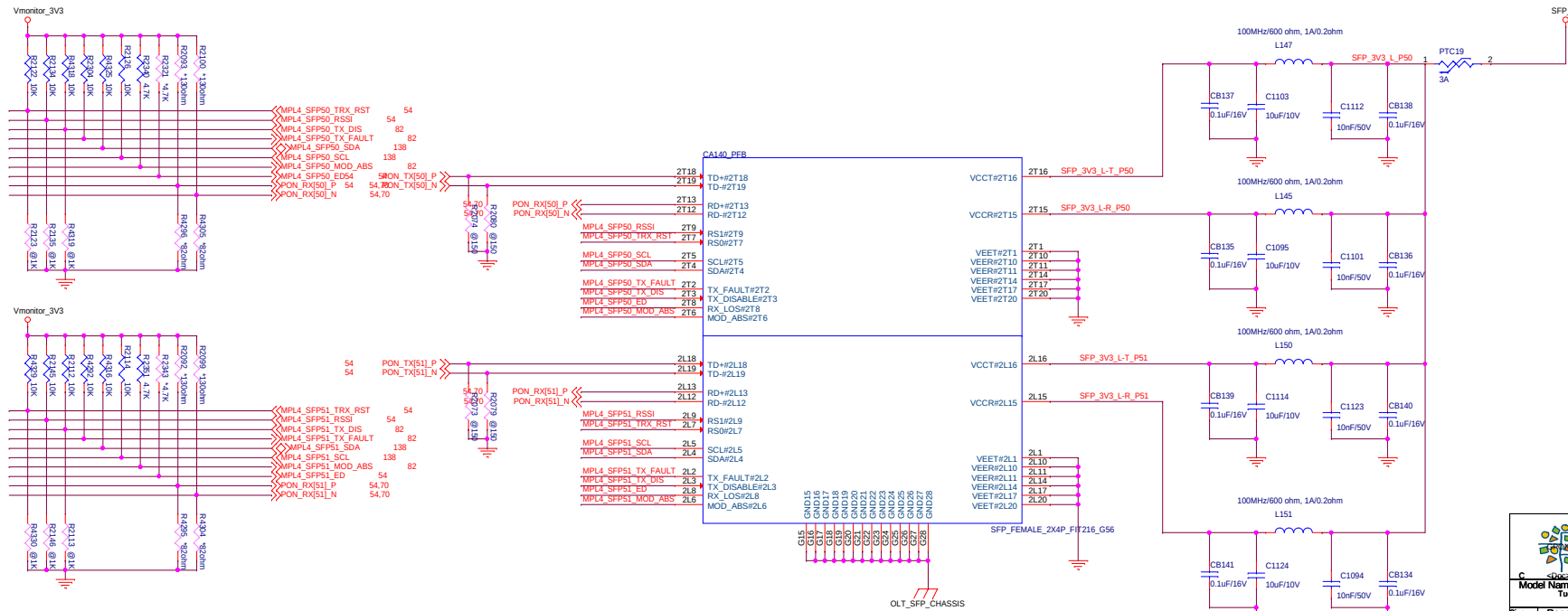


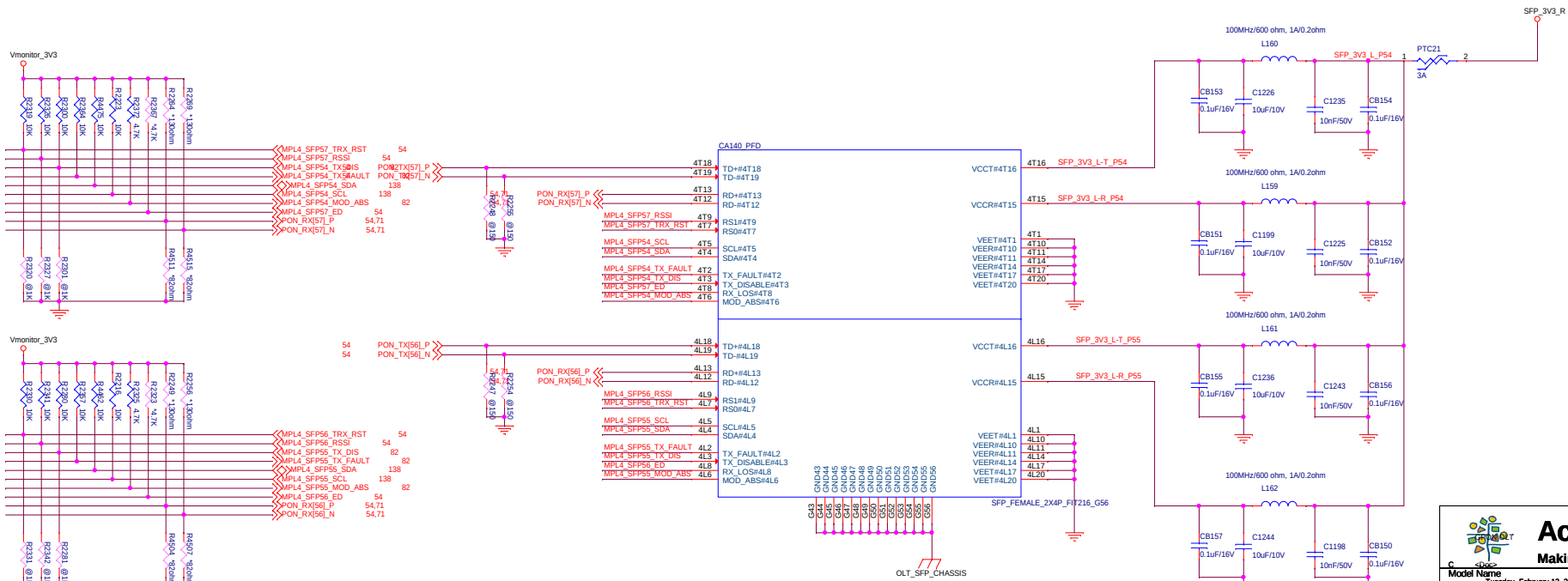
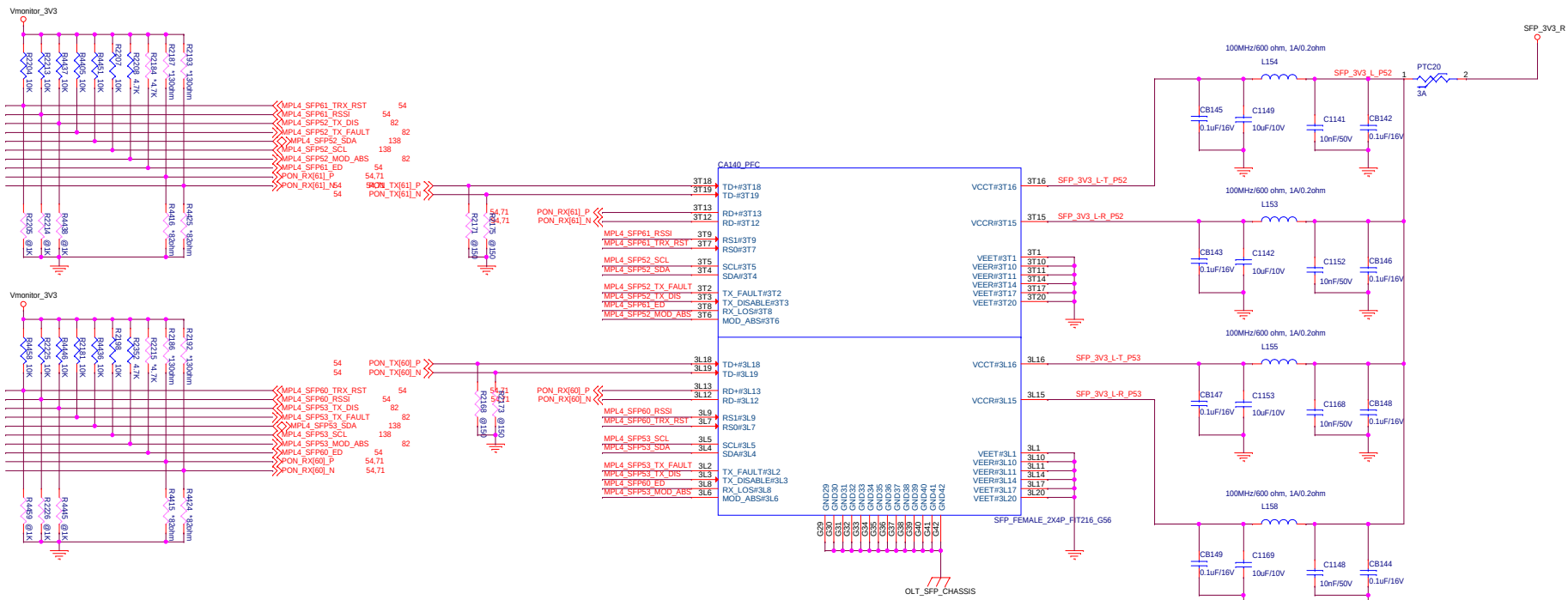


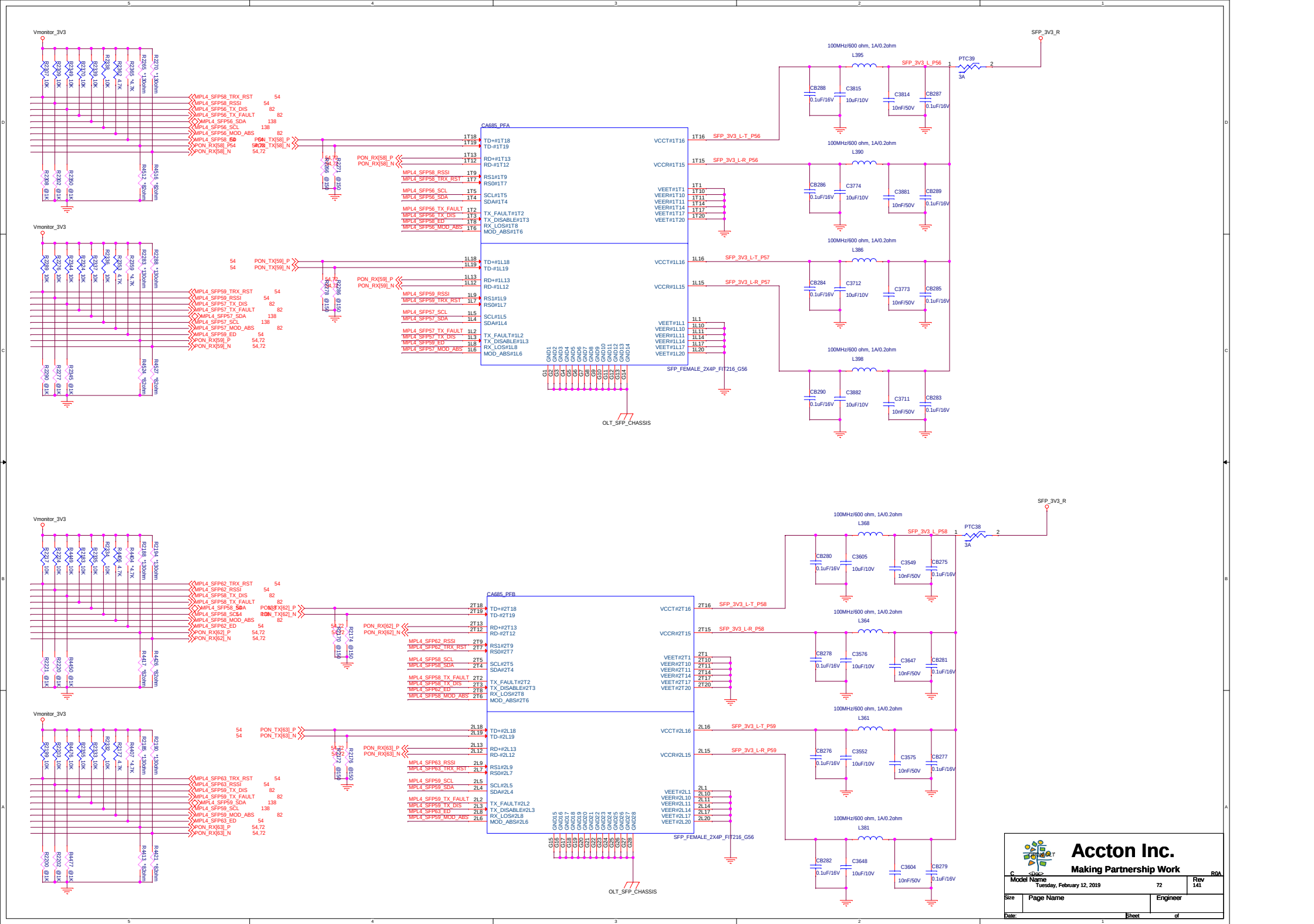


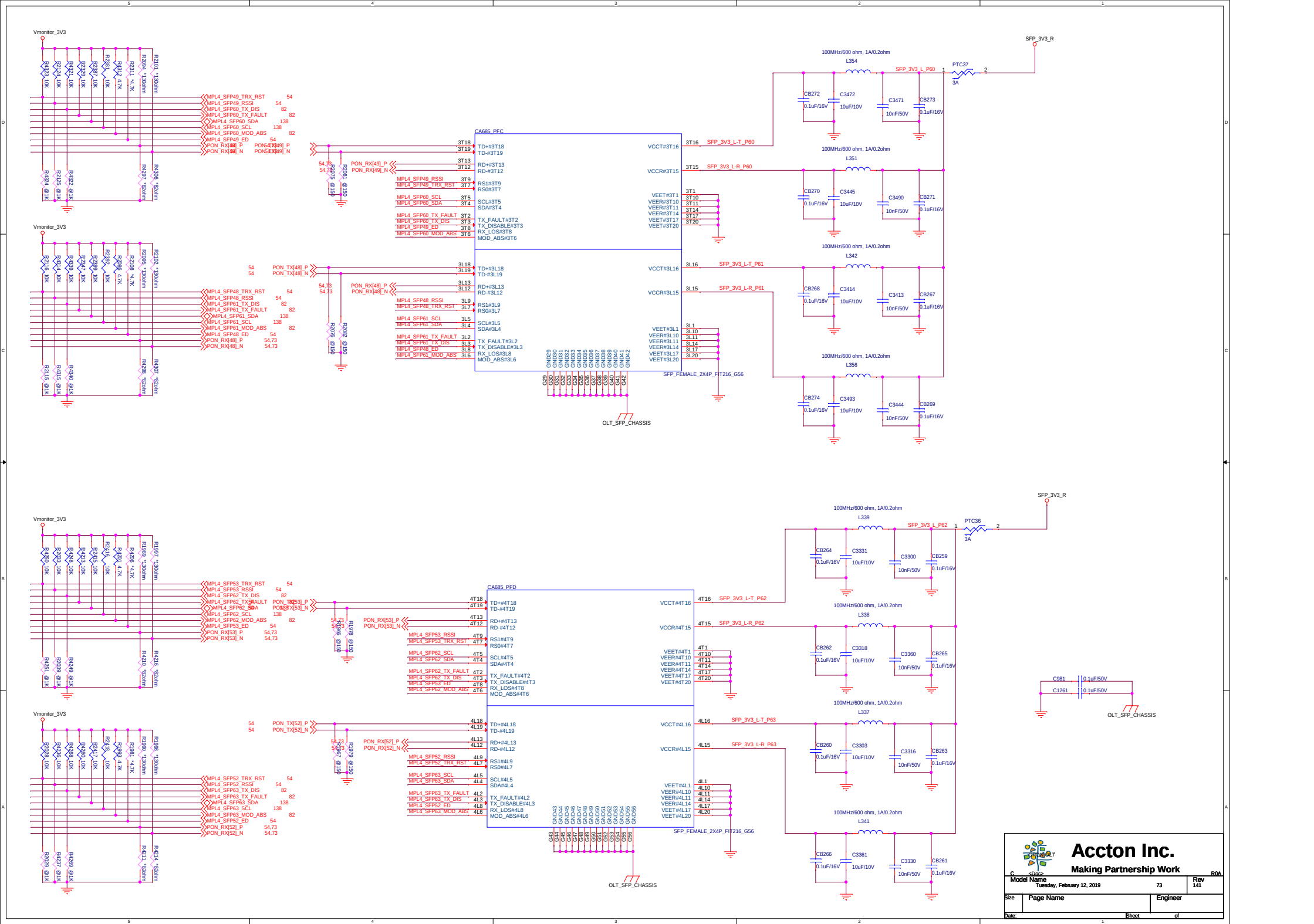




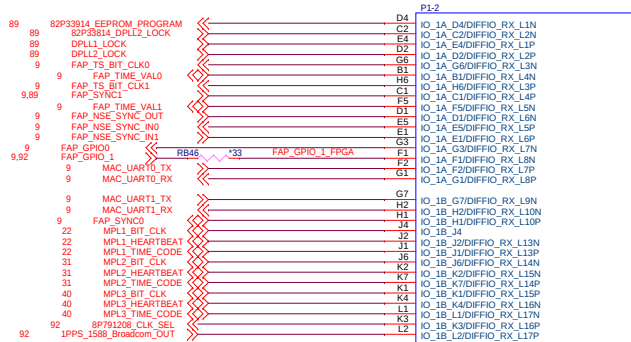








Bank2 is 2.5V level



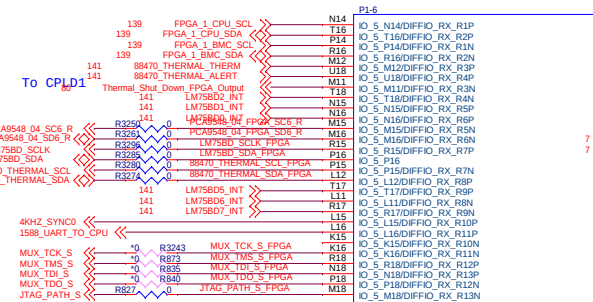
```
8P791208_CLK_SEL :
1 : Broadcom 1PPS
0:  IDT 1PPS
```

10M08DC U324
VERSION : 1.1
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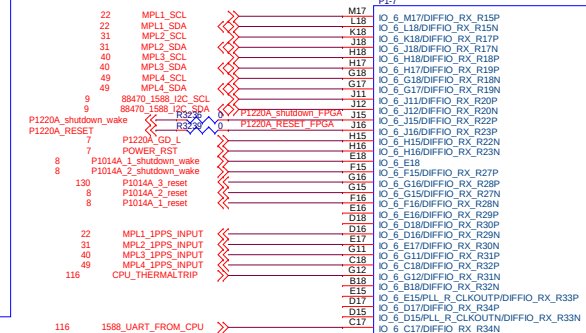
LM75BD2_INT : Thermal sensor from Main board

88470_THERMAL_ALERT : Thermal sensor from Main board 88470

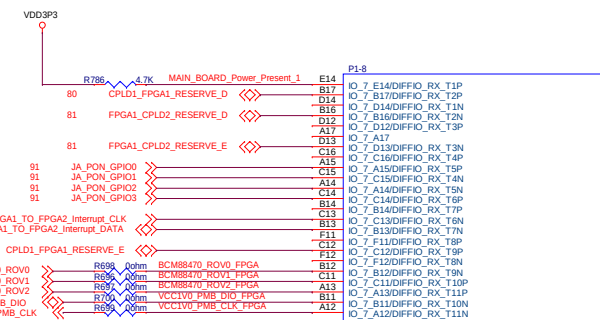
```
88470_THERMAL_THERM : Thermal sensor from Main board 88470
```



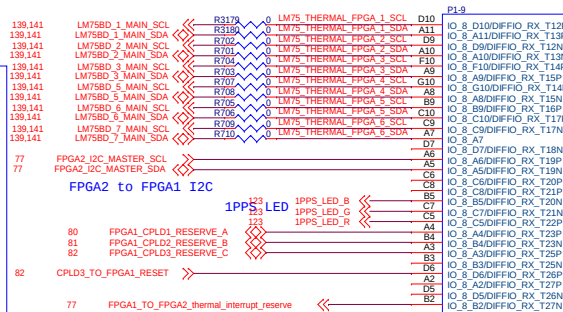
10M08DC U324
VERSION : 1.1
PAGE : 6 of 13
DATE : JAN_2017



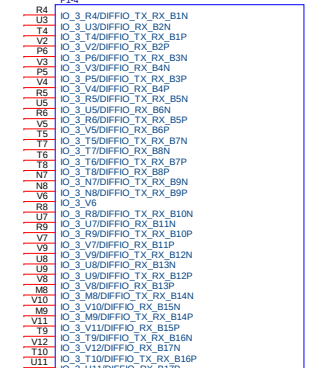
10M08DC U324
VERSION : 1.1
PAGE : 7 of 13
DATE : JAN_2017



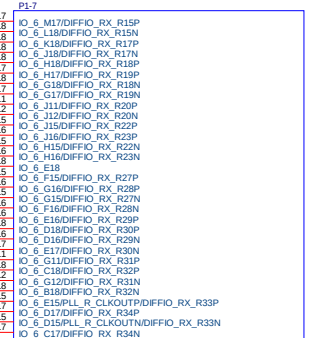
10M08DC U324
VERSION : 1.1
PAGE : 8 of 13
DATE : JAN_2017



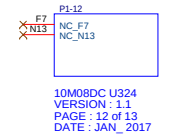
10M08DC U324
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10M08DC U324
VERSION : 1.1
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DATE : JAN_2017



10M08DC U324
VERSION : 1.1
PAGE : 7 of 13
DATE : JAN_2017



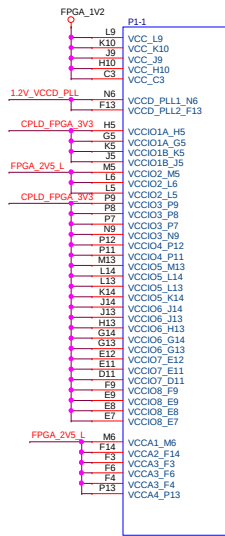
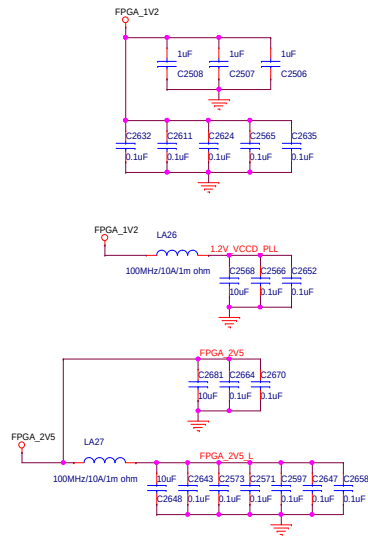
10M08DC U324
VERSION : 1.1
PAGE : 12 of 13
DATE : JAN_2017



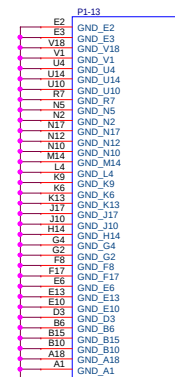
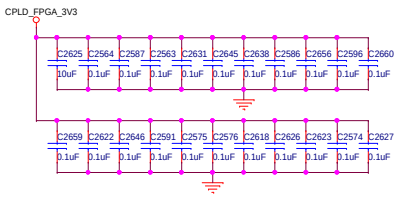
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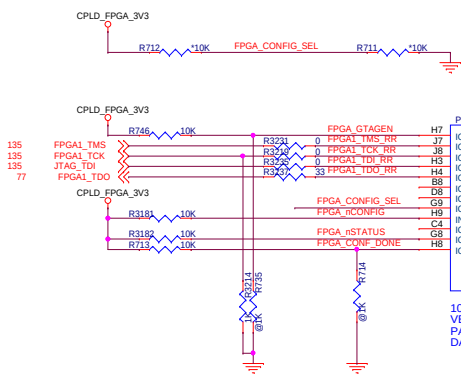
Model Name		74	Rev 141
Size	Page Name		Engineer



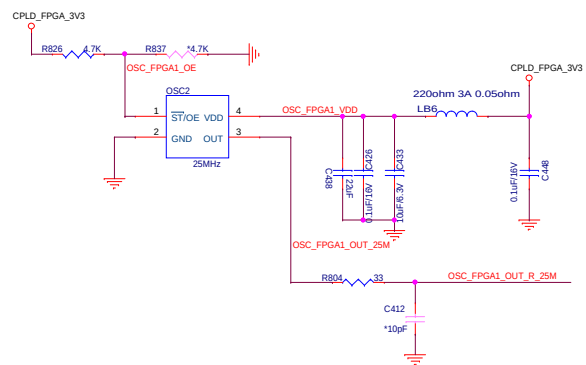
10M08DC U324
VERSION: 1.1
PAGE: 1 of 13
DATE: JAN_2017



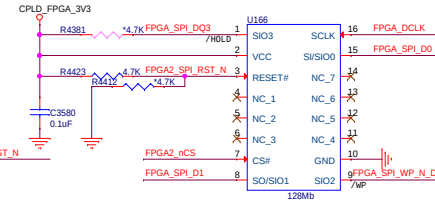
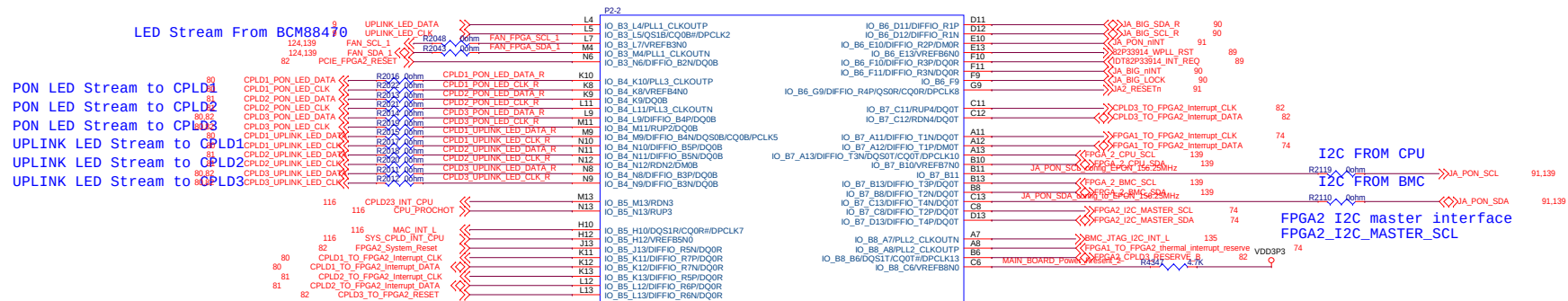
10M08DC U324
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Main board present signal



FPGA2_NCE0:
Low: Configure complete
(open drain output)

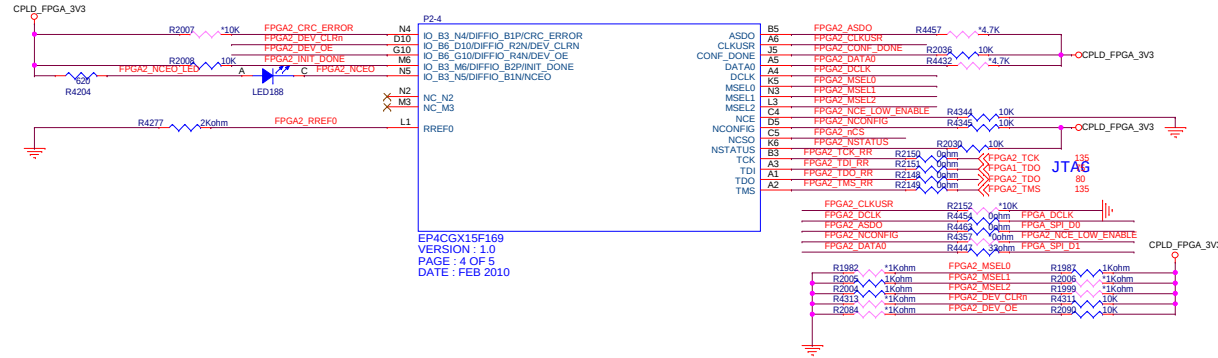


Table 8-3. Configuration Schemes for Cyclone IV GX Devices (EP4CGX15, EP4CGX22, and EP4CGX30 [except for F484 Package])

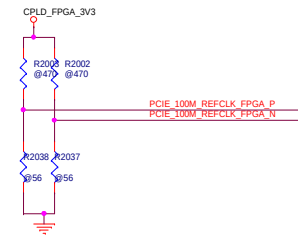
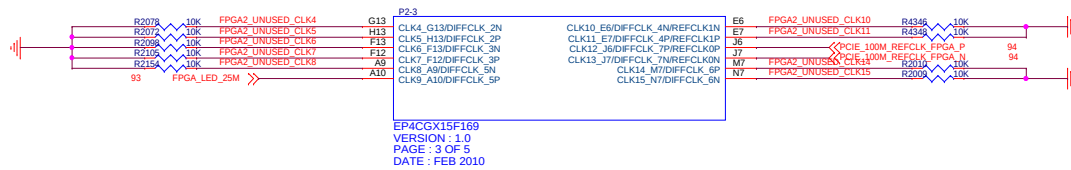
Configuration Scheme	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) (1)
AS	1	0	1	Fast	3.3
	0	1	1	Fast	3.0, 2.5
	0	0	1	Standard	3.3
PS	0	1	0	Standard	3.0, 2.5
	1	0	0	Fast	3.3, 3.0, 2.5
	1	1	0	Fast	1.8, 1.5
JTAG-based configuration (1)	0	0	0	Standard	3.3, 3.0, 2.5
JTAG-based configuration (1)	(1)	(1)	(1)	—	—

Notes to Table 8-3:

- (1) Configuration voltage standard applied to the V_{CC} supply of the bank in which the configuration pins reside.
- (2) JTAG-based configuration takes precedence over other configuration schemes, which means the nSTATUS pin settings are ignored.
- (3) Do not leave the nSTATUS pin floating. Connect them to V_{CC} or GND. These pins support the non-JTAG configuration scheme used in production. Always recommend connecting the nSTATUS pins to GND if your device is only using JTAG configuration.

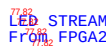
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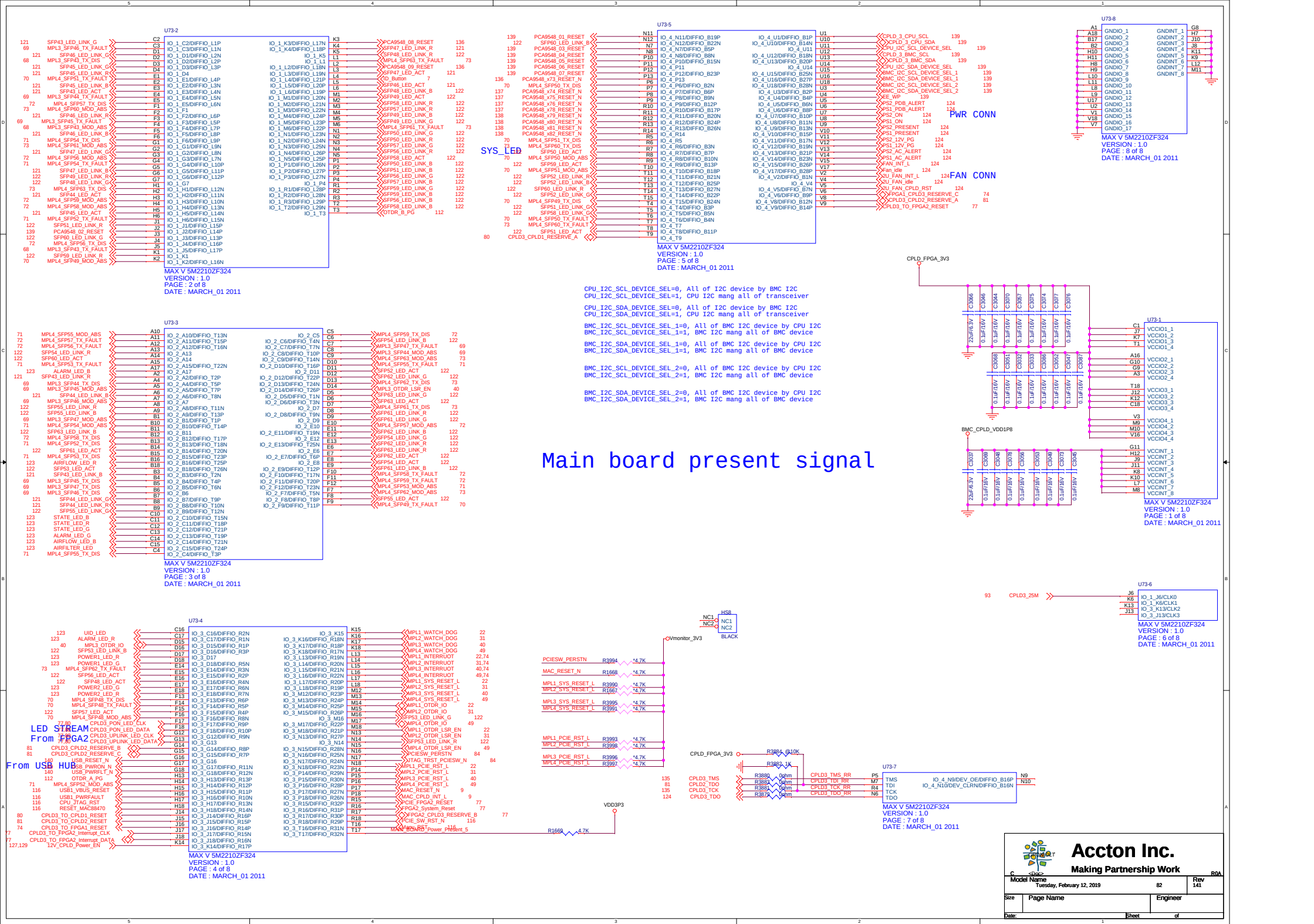


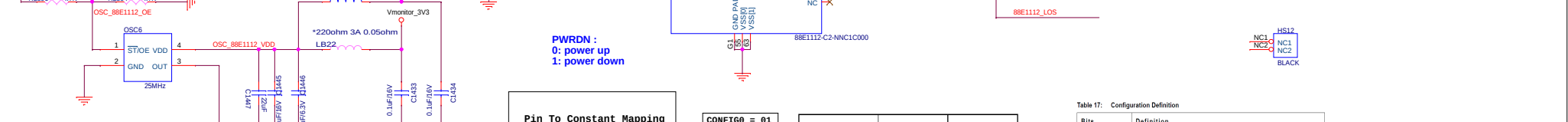
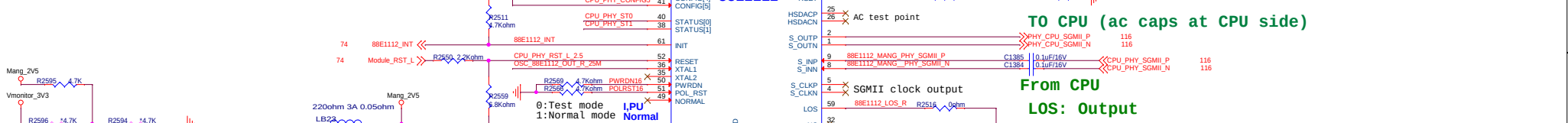
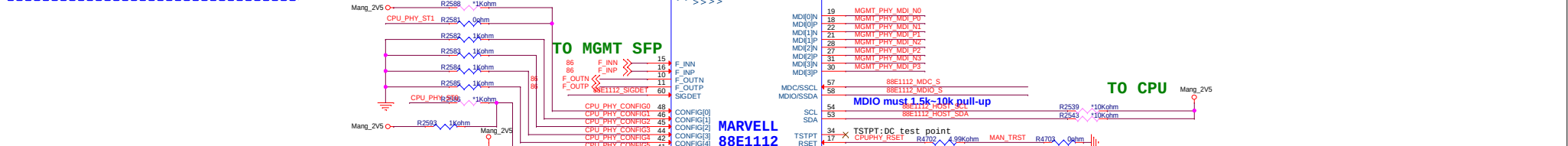
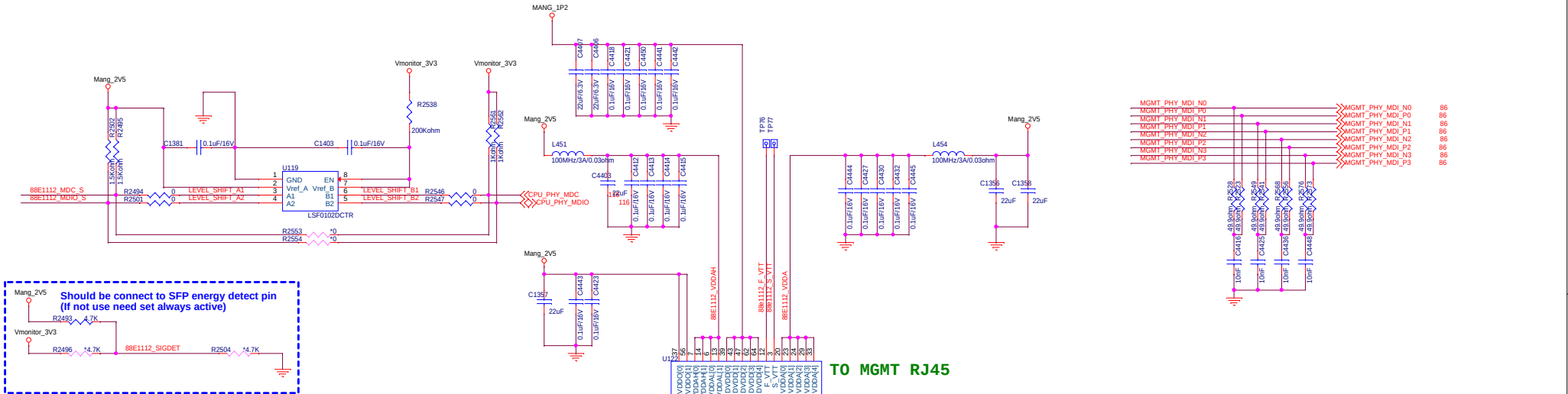
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Bits	Definition
PHYADR[4:0]	PHY Address
SGMII_CLK	0 = S_CLKPIN off 1 = S_CLKPIN active
EEPROM[1:0]	00 = No EEPROM Read 01 = Start reading from address 0 10 = Start reading from address 96 11 = Start reading from address 128
SEL_TWSI	0 = MDC/MDIO 1 = Two Wire Serial Interface
SEL_VTT	0 = F_VTT and S_VTT are internally regulated (Leave F_VTT and S_VTT floating) 1 = F_VTT and S_VTT are externally powered
MODE[0:1]	00 = SGMII MAC Interface to 100BASE-FX 01 = GBC to Copper 10 = SGMII MAC Interface to Auto media select (Copper/SGMII Media Interface) 11 = SGMII MAC Interface to Auto media select (Copper/1000BASE-X)

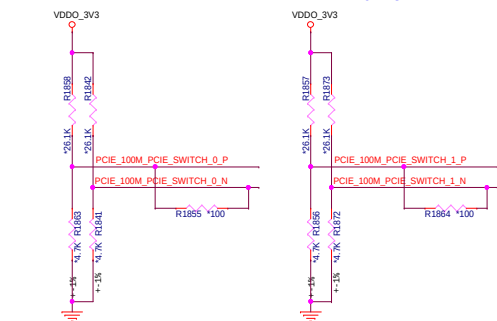
Register	Pin	Definition
16_3_15.12	LOS Control	0000 = Normal LOS operation 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Activity, Off - No Link 0011 = On - Link, Blink - Activity, Off - No Link 0100 = On - Link, Blink - Activity, Off - No Link 0101 = On - Link, Blink - Activity, Off - No Link 0110 = On - Link, Blink - Activity, Off - No Link 0111 = On - Link, Blink - Activity, Off - No Link 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Register	Pin	Definition
16_3_15.12	LOS Control	0000 = Normal LOS operation 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Activity, Off - No Link 0011 = On - Link, Blink - Activity, Off - No Link 0100 = On - Link, Blink - Activity, Off - No Link 0101 = On - Link, Blink - Activity, Off - No Link 0110 = On - Link, Blink - Activity, Off - No Link 0111 = On - Link, Blink - Activity, Off - No Link 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

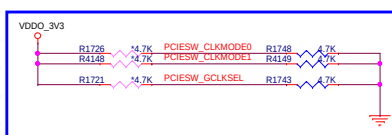
[illegible]

STPFS Field in the STPFS Data		Block Configuration						
Hex	Binary	P33	P32	P31	P30	P18	P17	P16
0x0	00000000							x8
0x1	00000001							x8
0x2	00000010	x2						x8
0x3	00000011	x2					x2	
0x4	00000100					x4	x2	x2
0x5	00000101					x4	x2	x2
0x6	00000110					x4	x1	x1 x1
0x7	00000111					x4	x1	x1 x1
0x8	00001000							x2
0x9	00001001							x2
0xA	00001010	x2					x1	x1
0xB	00001011	x2					x1	x1
0xC	00001100	x1	x1					x2
0xD	00001101	x1	x1					x2
0xE	00001110	x2	x1	x1				x2
0xF	00001111	x1	x2	x1	x1			x2
0x10	00100000							x1
0x11	00100001							x1
0x12	00100010	x1	x1	x2	x1	x1	x1	x1
0x13	00100011	x1	x1	x2	x1	x1	x1	x1
0x14	00100100	x1	x1	x1	x1	x1	x1	x2
0x15	00100101	x1	x1	x1	x1	x1	x1	x2
0x16	00100110	x1	x1	x1	x1	x1	x1	x1
0x17	00100111	x1	x1	x1	x1	x1	x1	x1
0x18	00101000							x2

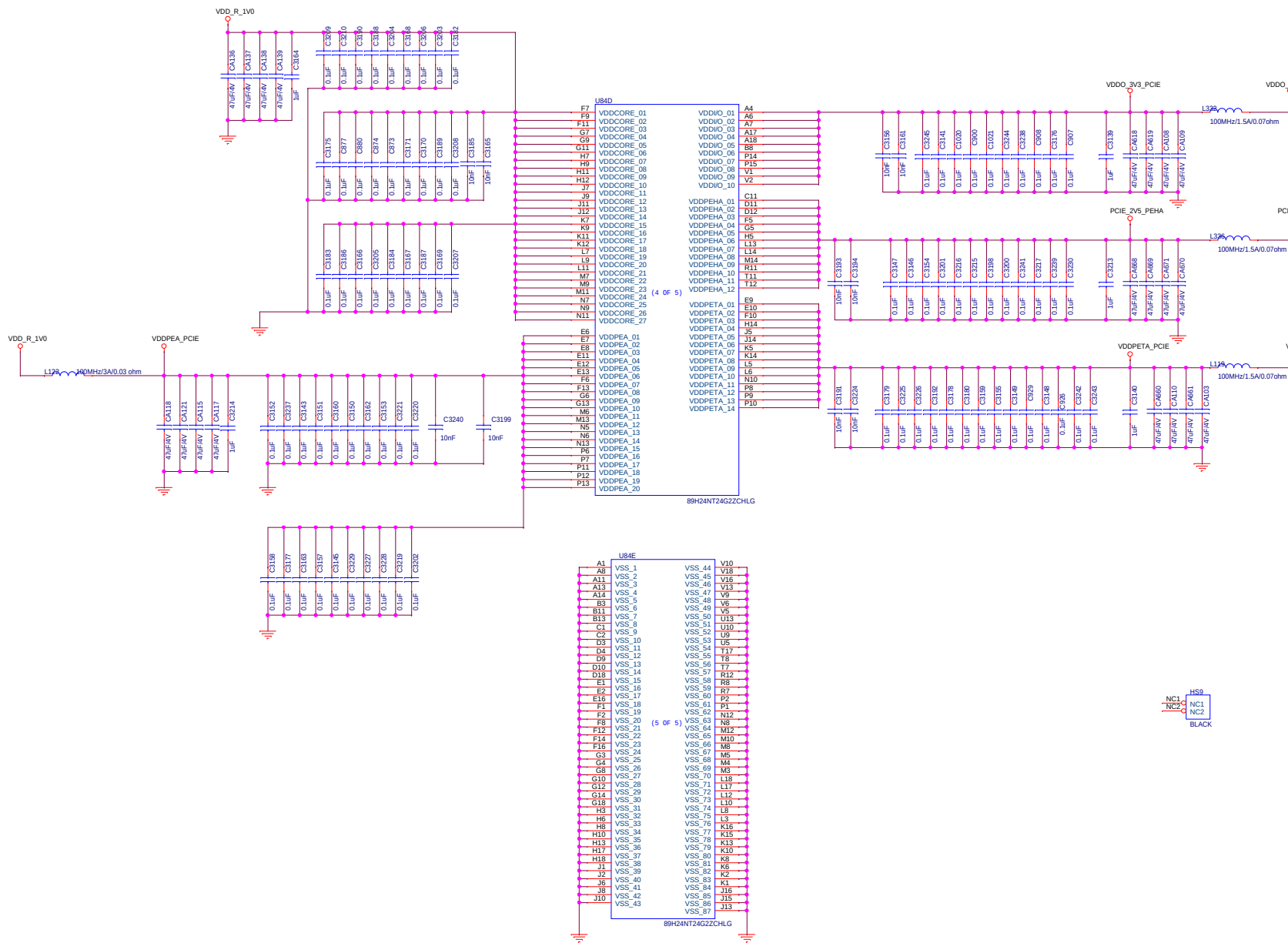
Table 3. Possible Configurations for Block 3 (Sheet 1 of 2)

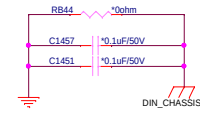
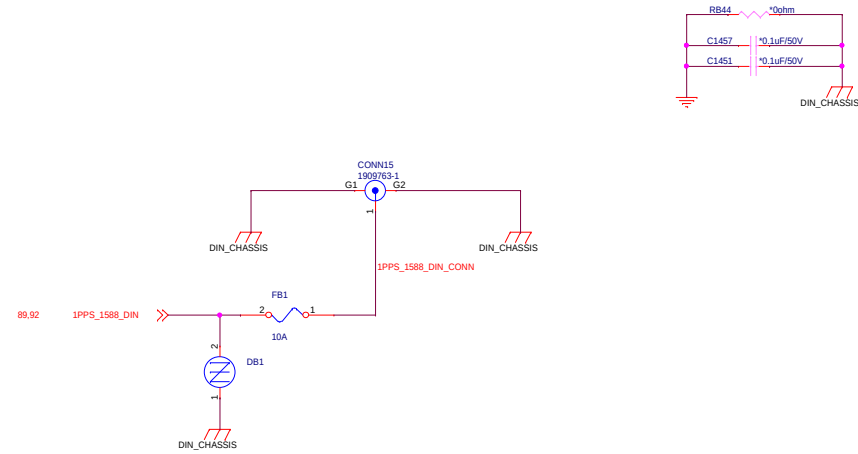
Table 12.17 Slave SMBus Address

CLKMODE[1:0] Value in Boot Configuration Vector	Port 0 Clocking Mode	Port 0 SCLK	Port 0 MCLK
0	Global Clock	0 (non-common clock)	0 (non-common clock)
1	Global Clock	1 (common clock)	0 (non-common clock)
2	Global Clock	0 (non-common clock)	1 (common clock)
3	Global Clock	1 (common clock)	1 (common clock)



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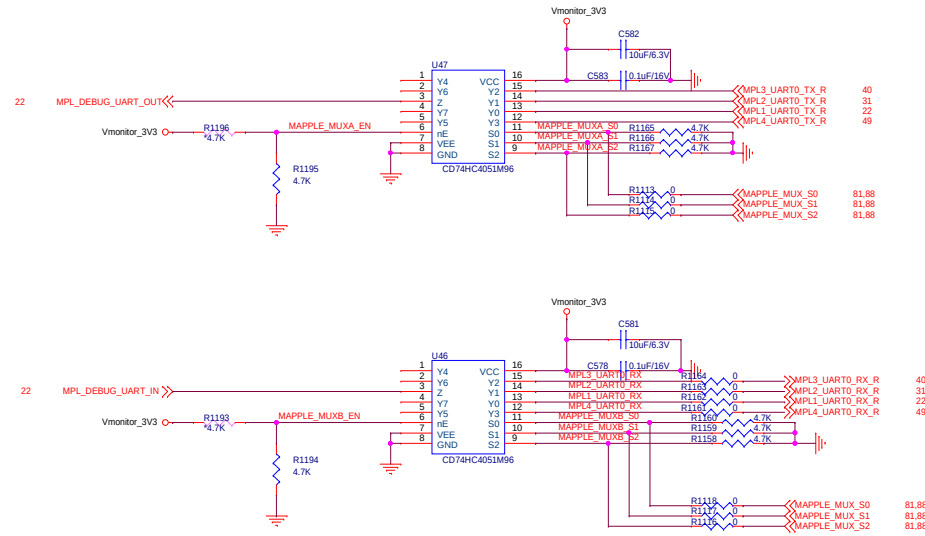
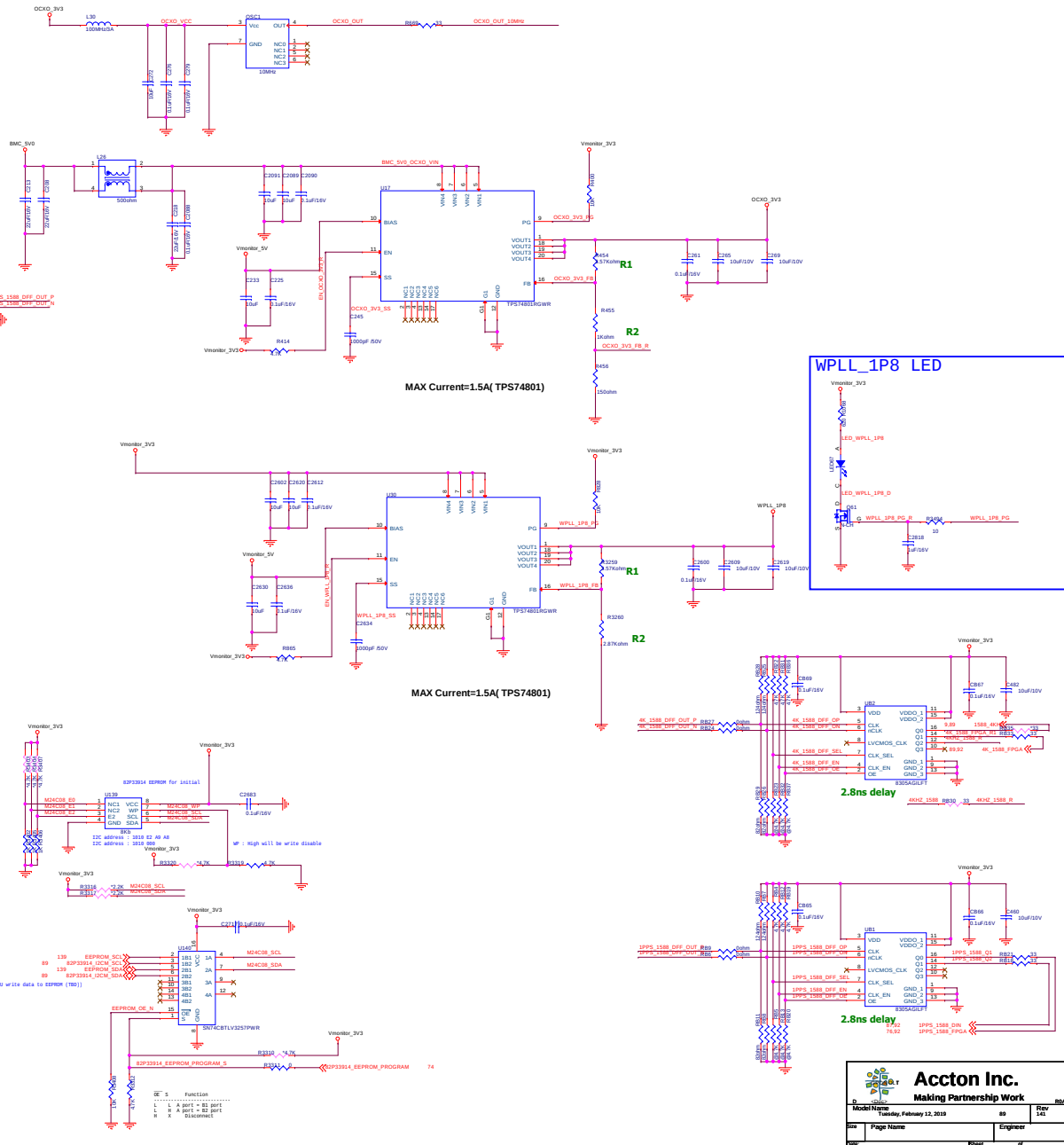
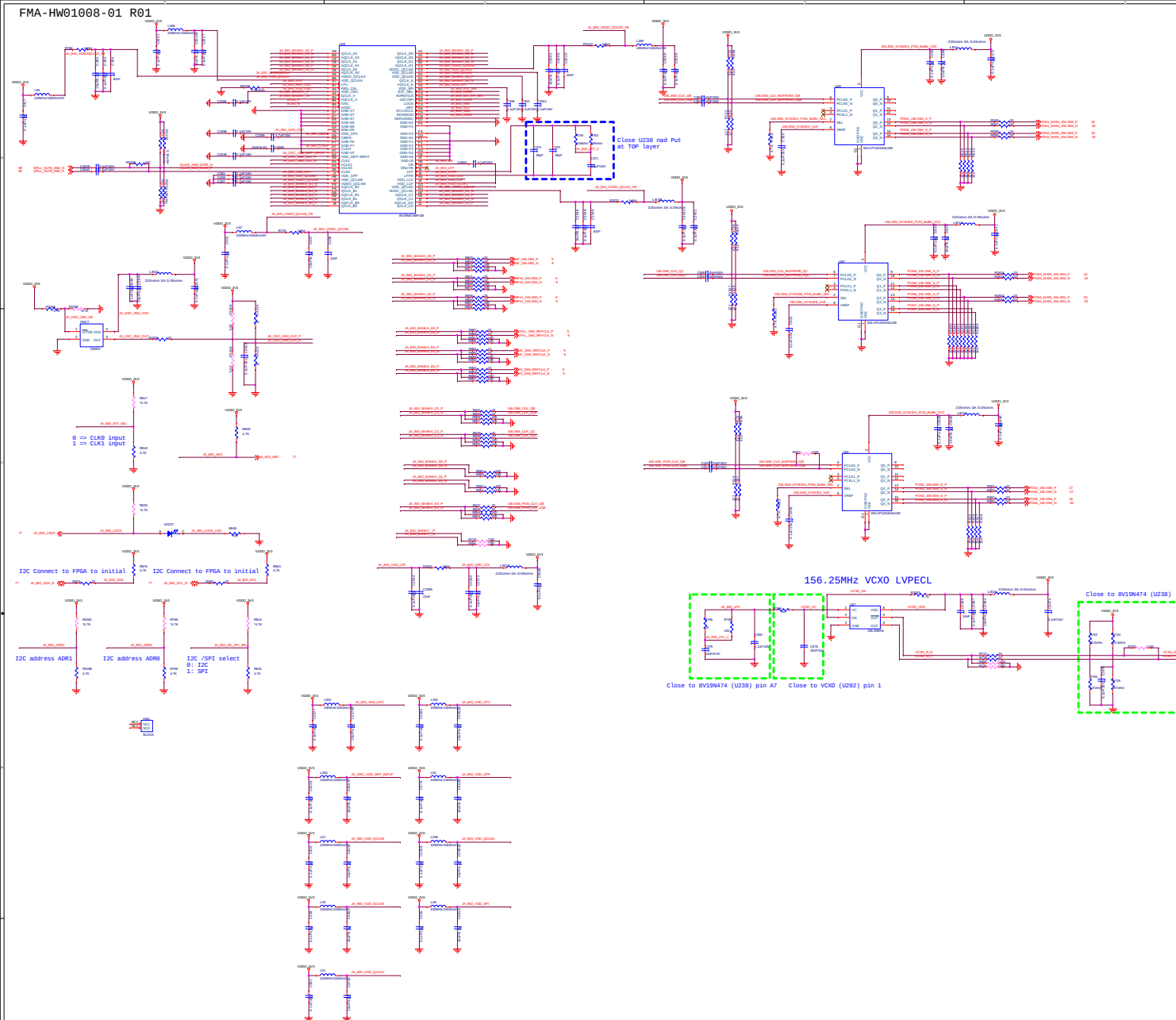


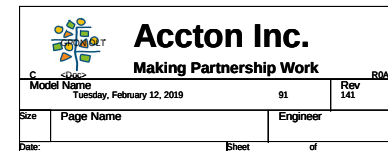
Table 1. TRUTH TABLE
'HC/CD74HCT4051⁽¹⁾

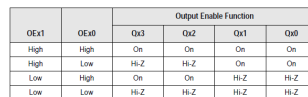
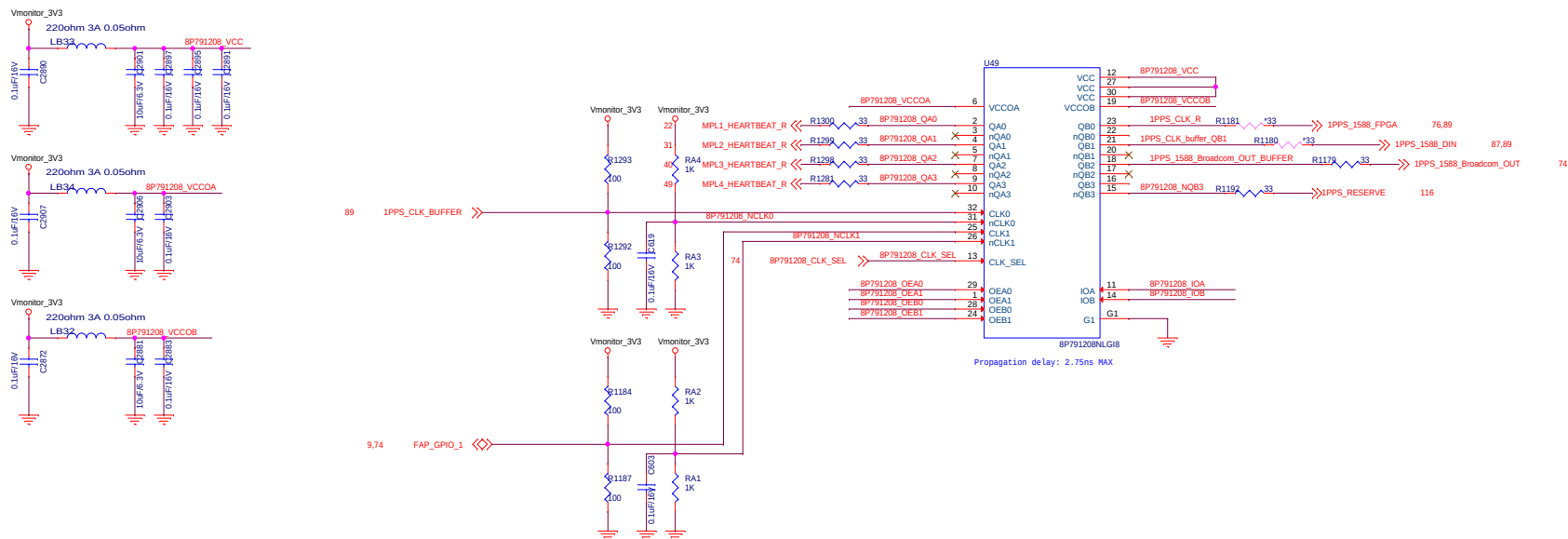
INPUT STATES				ON CHANNELS
ENABLE	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

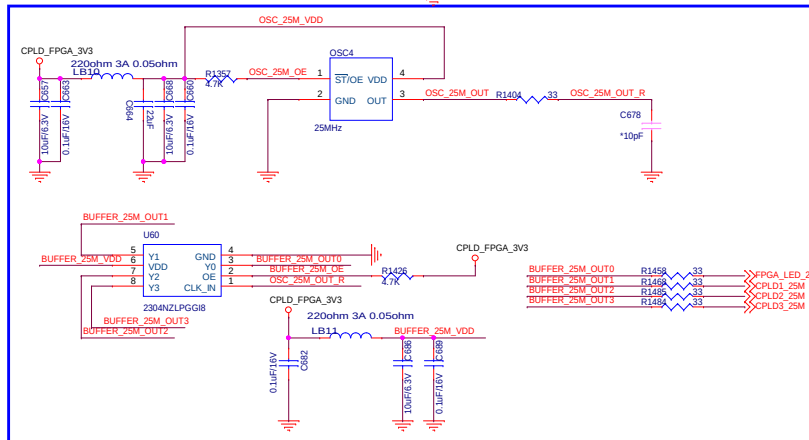
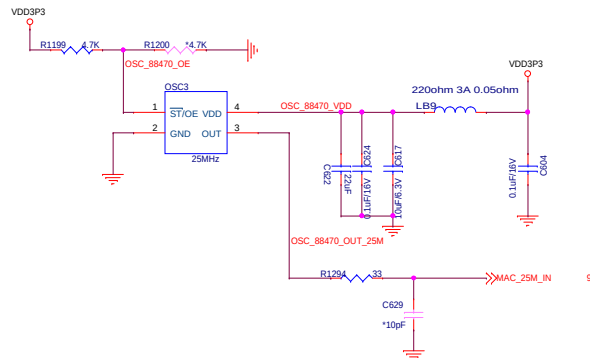
(1) X = Don't care











79
80
81
82

FMA-HW01008-01 R01

PCIe Buffer for PON

PLL Operating Mode

HIBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

1=> HIBW
 0=> LOBW
 MID=> BYPASS
 1=> Select 100MHz
 0=> Select 133.33MHz

1 = disable outputs,
 0 = enable outputs

AC coupled CAPS closed to 94XL0831

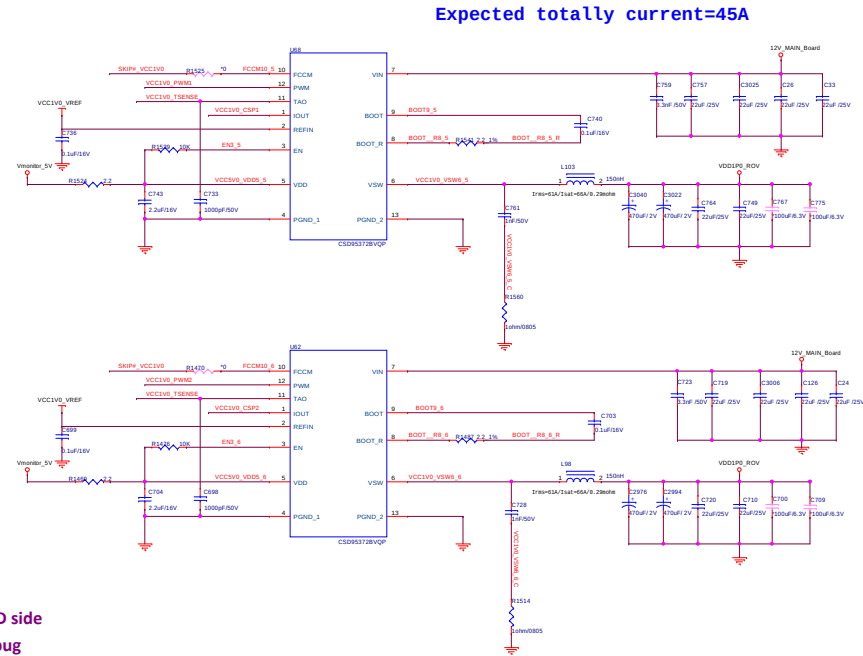
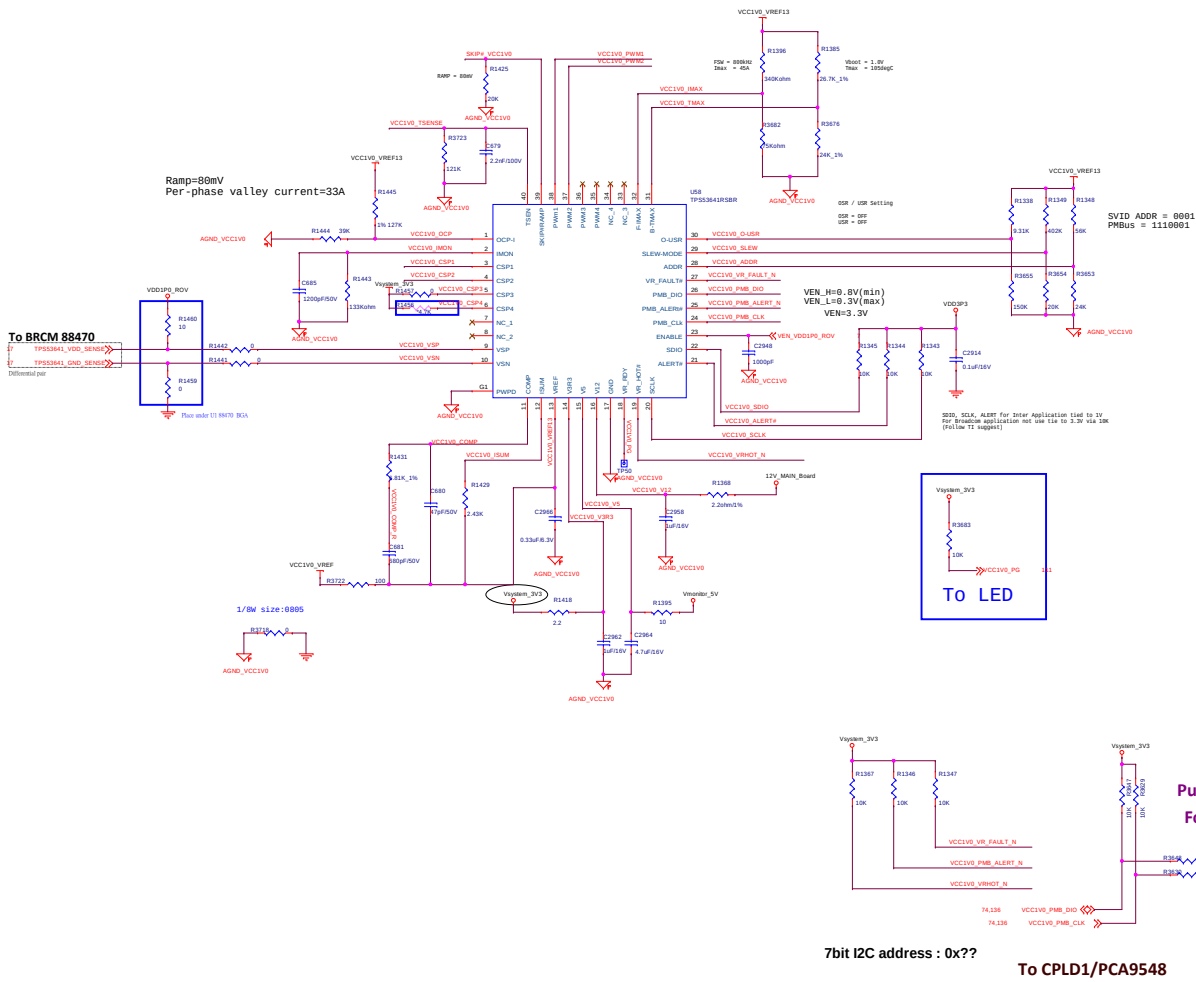


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VDD1P0_ROV/45A



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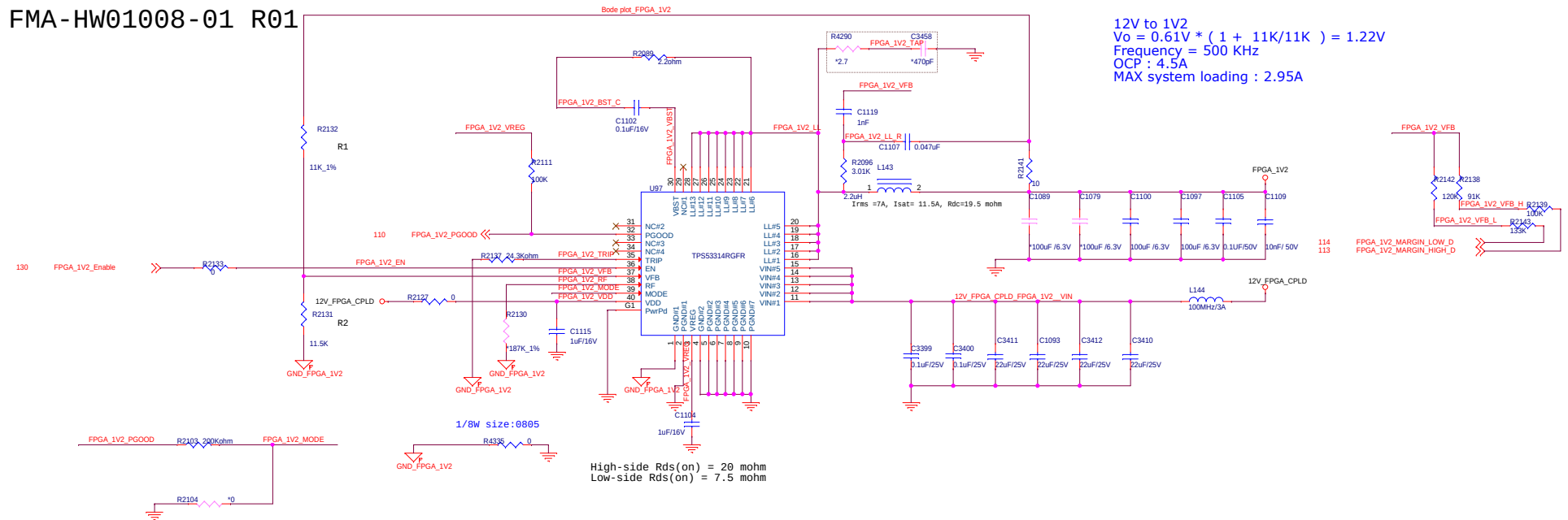
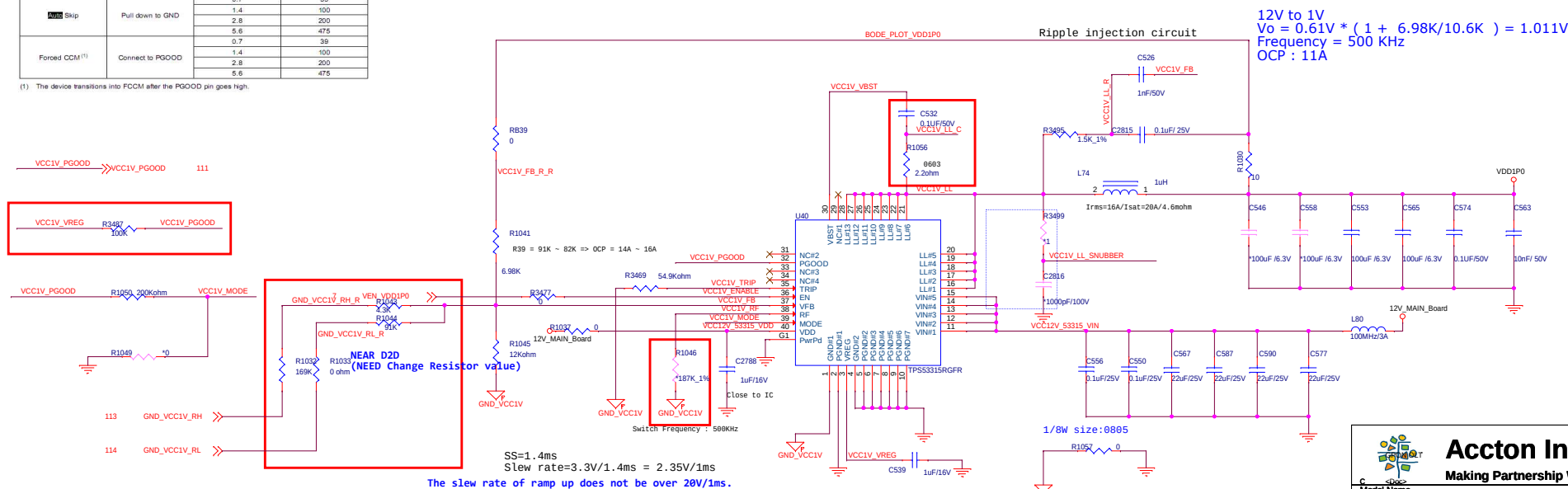


Table 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{POD} (kΩ)
POD Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

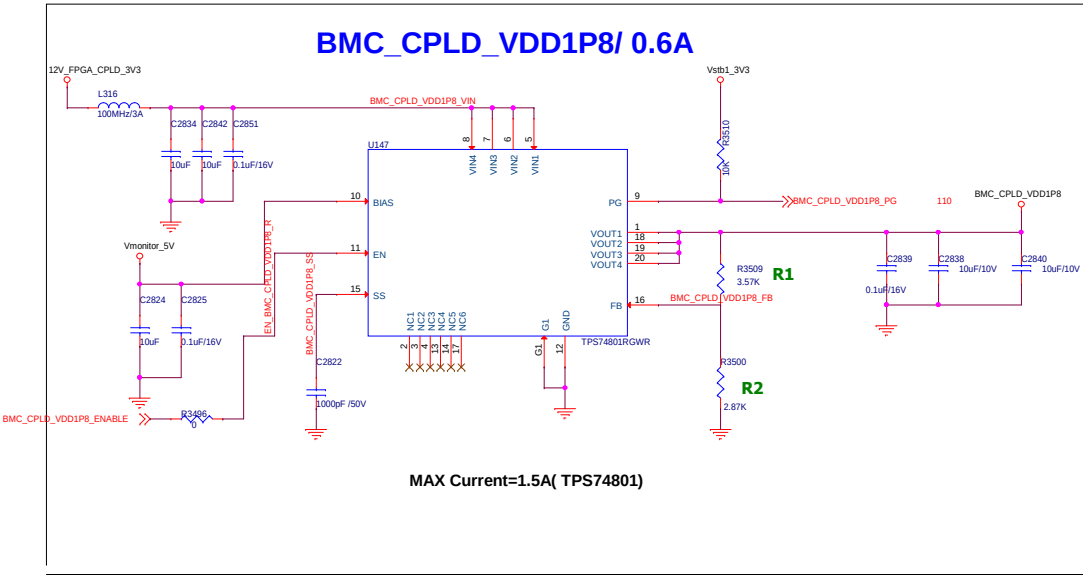
(1) The device transitions into FCCM after the PGOOD pin goes high.

VDD1P0/ 7.255A



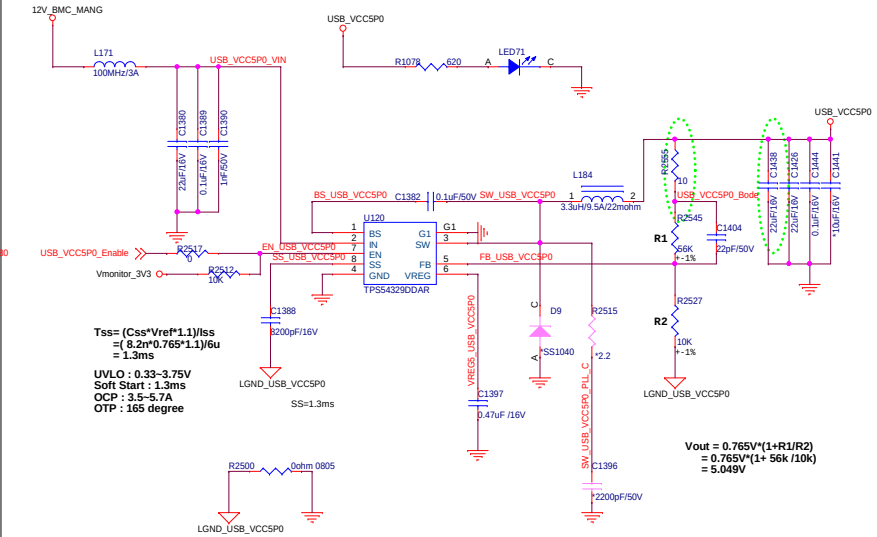
12V to 1V
 $V_o = 0.61V * (1 + 6.98K/10.6K) = 1.011V$
 Frequency = 500 KHz
 OCP : 11A

BMC_CPLD_VDD1P8/ 0.6A



MAX Current=1.5A(TPS74801)

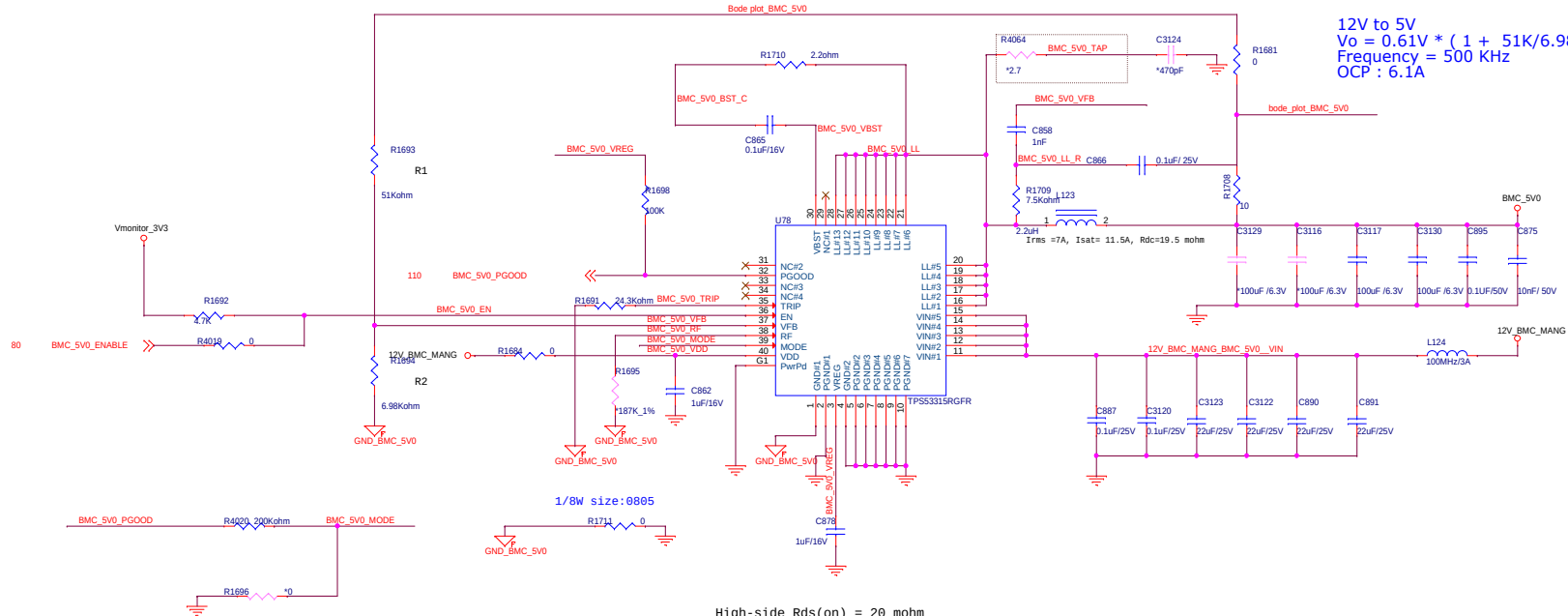
12V convert to 5V @1A For USB



$T_{ss} = (C_{ss} \cdot V_{ref} \cdot 1.1) / I_{ss}$
 $= (8.2nF \cdot 0.765V \cdot 1.1) / 6u$
 $= 1.3ms$
UVLO : 0.33-3.75V
Soft Start : 1.3ms
OCP : 3.5-5.7A
OTP : 165 degree

$V_{out} = 0.765V \cdot (1 + R1/R2)$
 $= 0.765V \cdot (1 + 56k/10k)$
 $= 5.049V$

BMC_5V0/ 4A



12V to 5V
 $V_o = 0.61V \cdot (1 + 51K/6.98K) = 5.067V$
Frequency = 500 kHz
OCP : 6.1A

High-side $R_{ds(on)} = 20 \text{ mohm}$
Low-side $R_{ds(on)} = 7.5 \text{ mohm}$

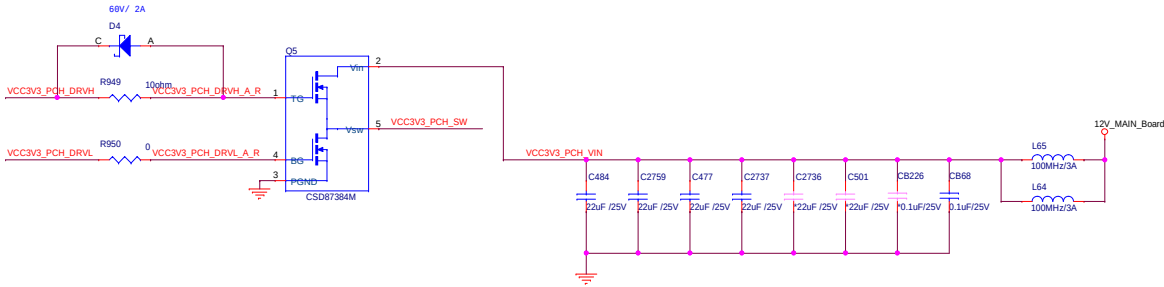
MODE: Auto-skip
 $V_{trip} (mV) = R_{trip} (Kohm) \cdot I_{trip} (uA)$
 $I_{ocp} = V_{trip} / (8 \cdot R_{ds(on)}) + I_{ind(ripple)} / 2 = 6.34 \text{ A}$

VDD3P3/ 13.482A

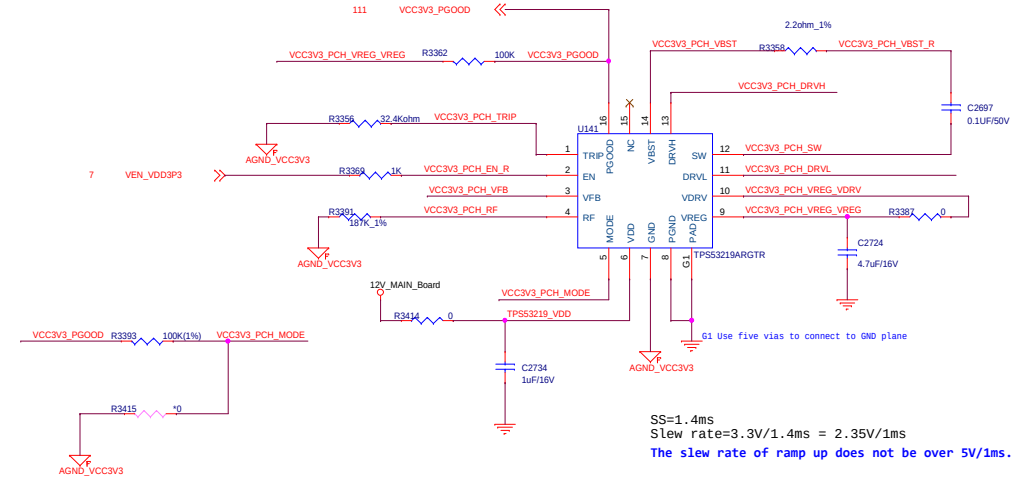
Table 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device goes into Forced CCM after PGOOD becomes high.

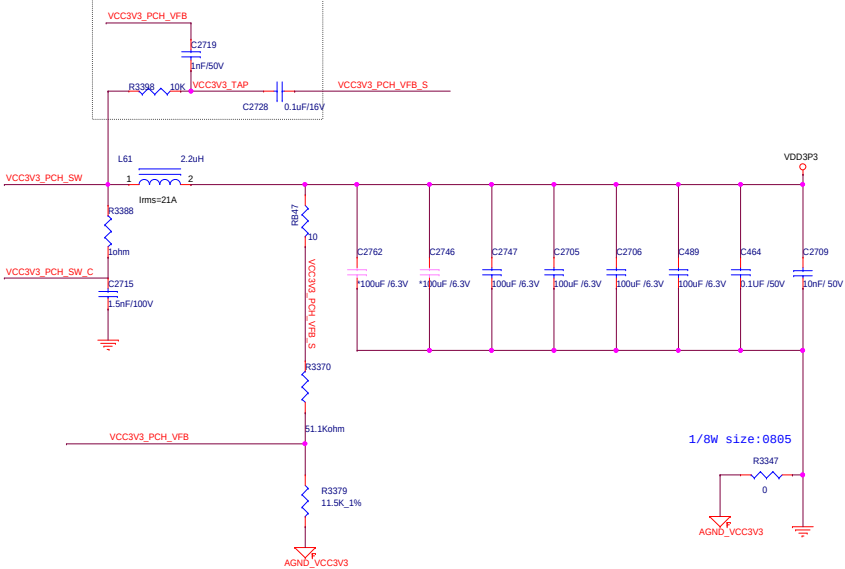


Vendor: TI
P/N: TP553219ARGTR
Accton: 11680000228A
Fsw: 300kHz



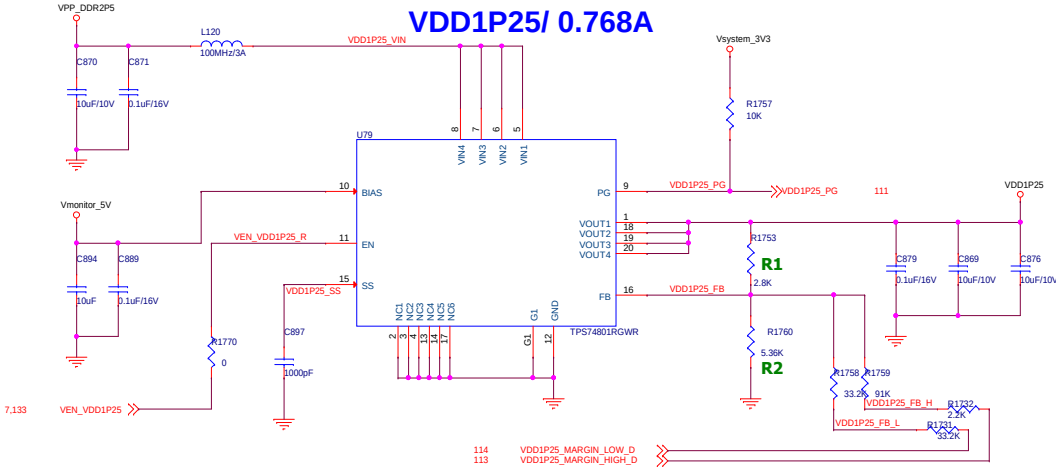
SS=1.4ms
Slew rate=3.3V/1.4ms = 2.35V/1ms
The slew rate of ramp up does not be over 5V/1ms.

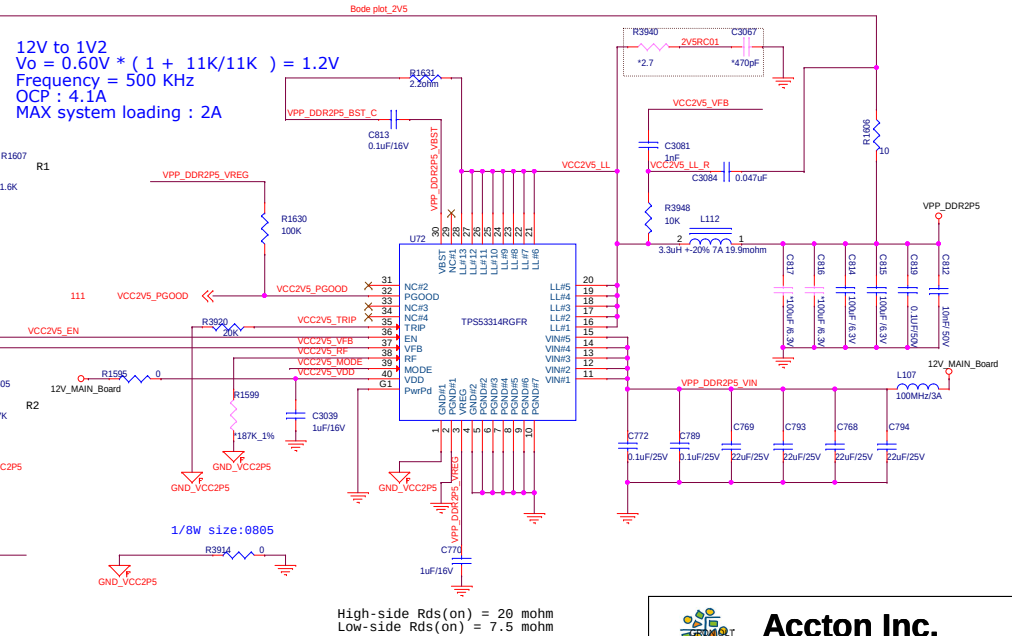
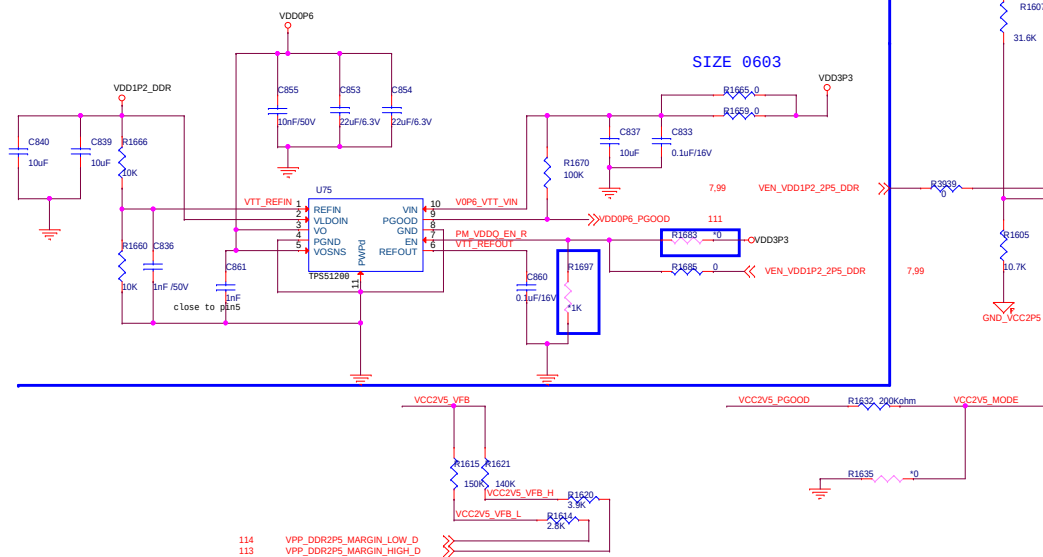
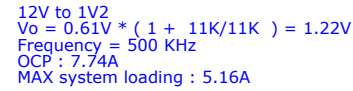
Ripple injection circuit

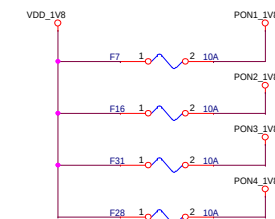
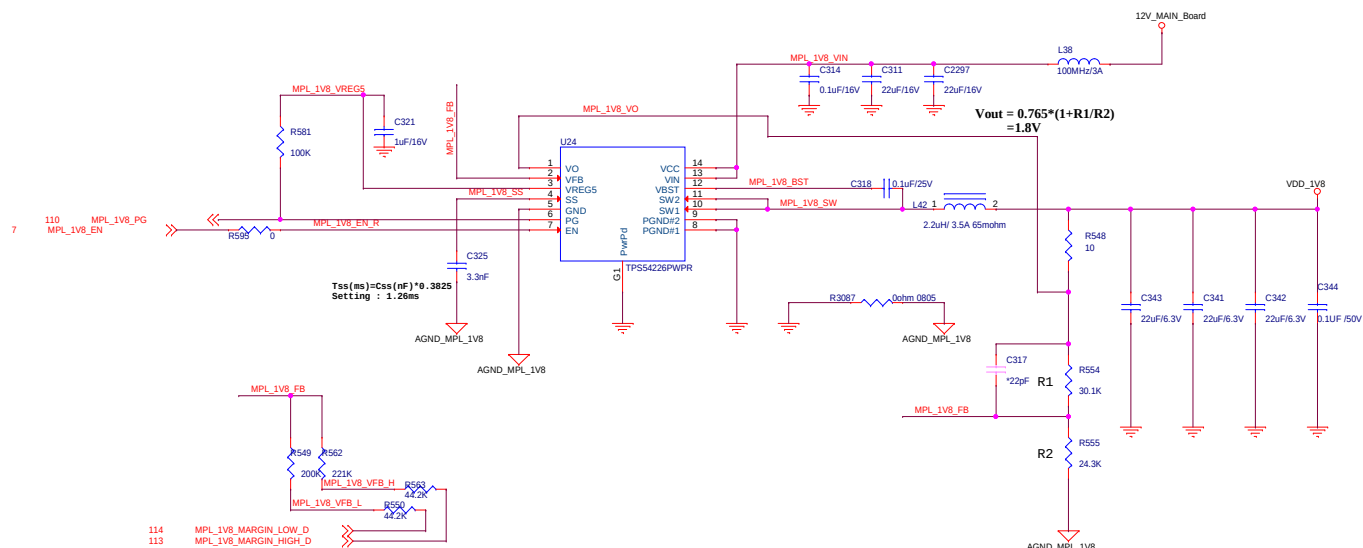
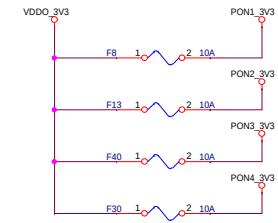


2.5V convert to 1.25V @1A For BCM88470

VDD1P25/ 0.768A




$$\text{Iocp} = \text{Vtrip} / (8 * \text{Rds(on)}) + \text{Iind(ripple)}/2 = 6.34 \text{ A}$$



FMA-HW01008-01 R01

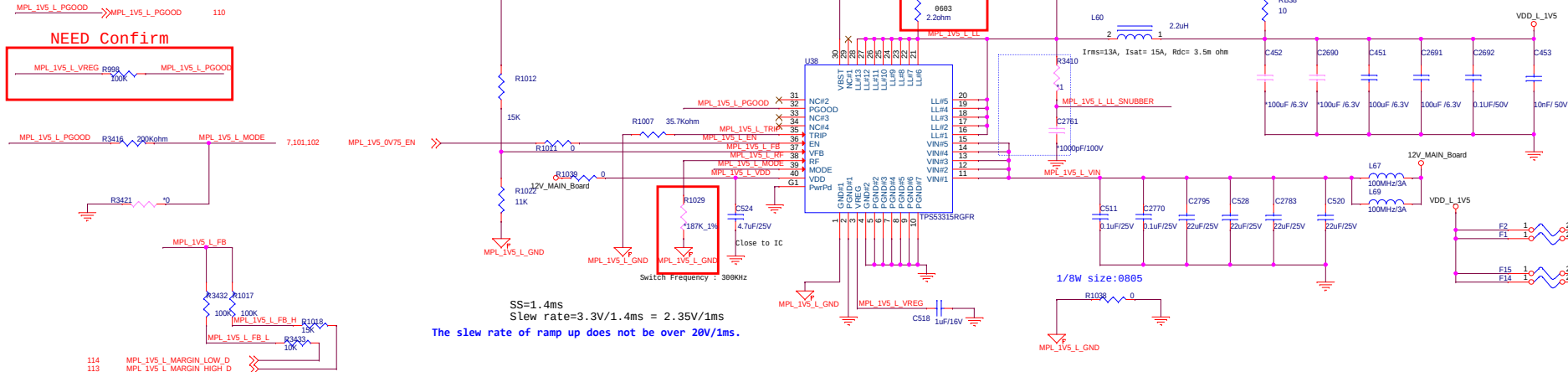
Table 1. Soft-Start and MOD

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{DSOFT} (kΩ)
Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) The device transitions into FCCM after the PGOOD pin goes high.

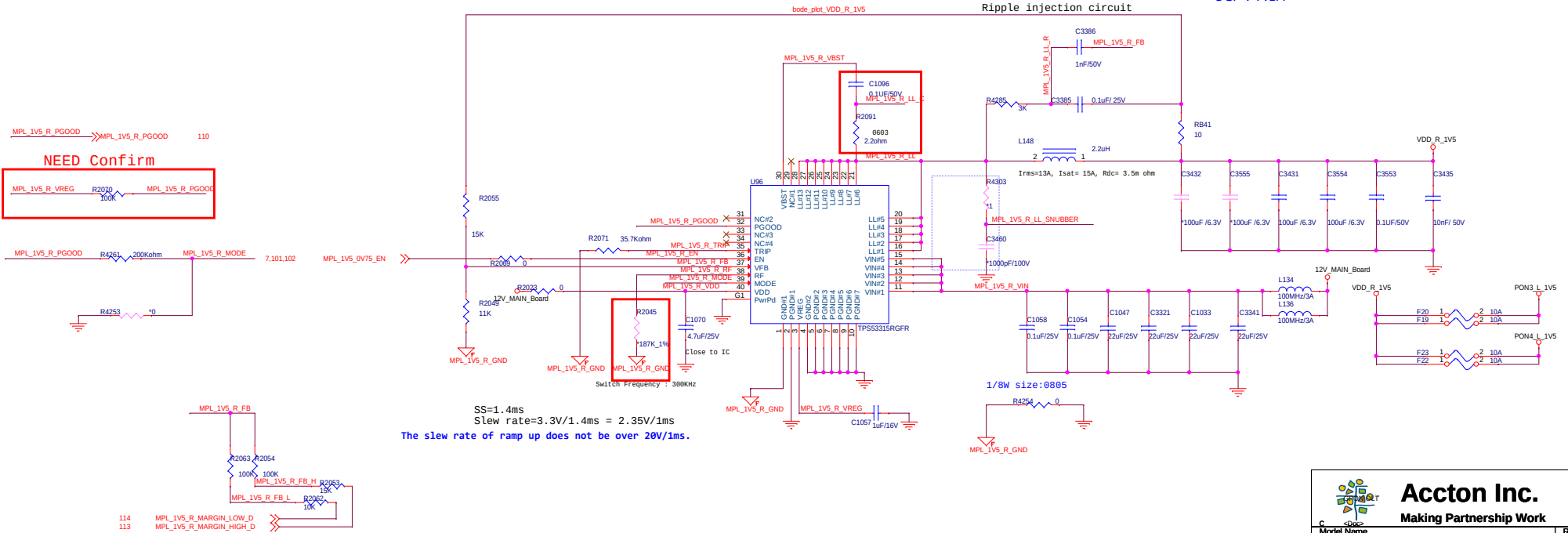
VDD_L_1V5/ 4.76A

12V to 1V
 $V_o = 0.607V * (1 + 15K/10K) = 1.518V$
 Frequency = 500KHz
 OCP : 7.1A



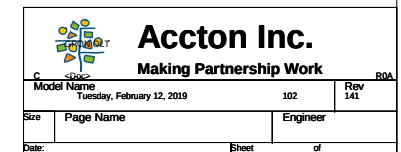
VDD_R_1V5/ 4.76A

12V to 1V
 $V_o = 0.607V * (1 + 15K/10K) = 1.518V$
 Frequency = 500KHz
 OCP : 7.1A

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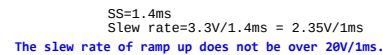
Making Partnership Work

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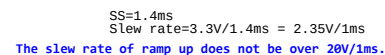
MODE SELECTION	ACTION	SOFT-START TIME (ms)	Ramp (kV)
Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

NEED Confirm



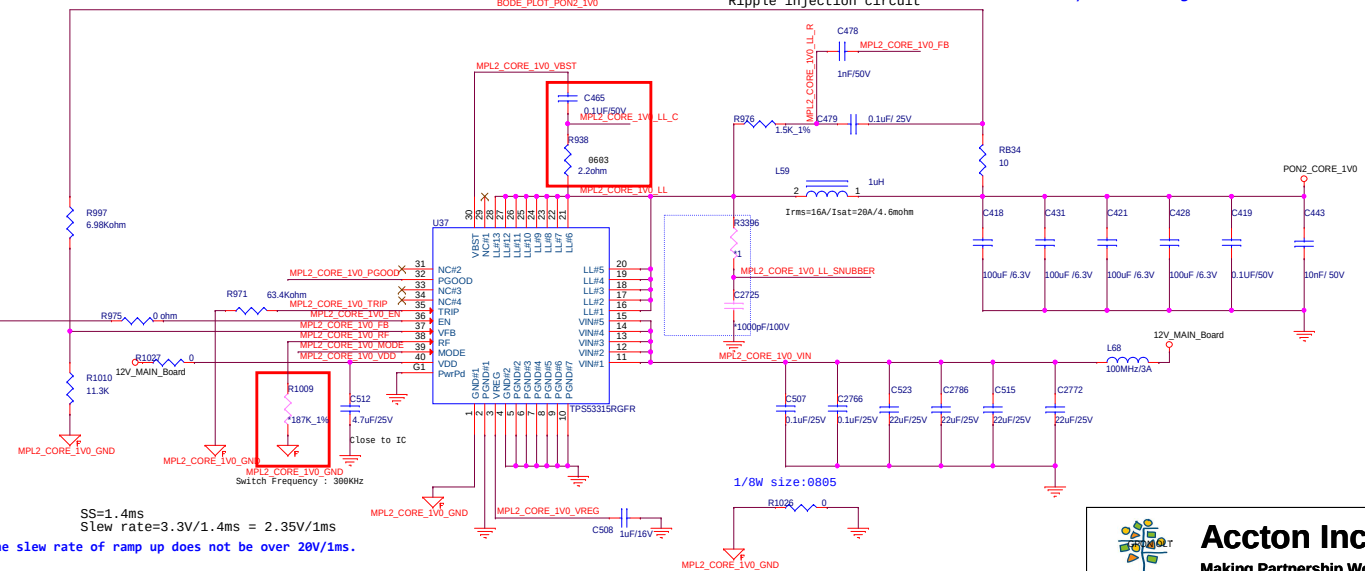
MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{DSOFT} (kΩ)
 Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

NEED Confirm



PON2_1V0/ 8.148A

BODE_PLOT_PON2_1V0 Ripple injection circuit



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12V to 1V
 $V_o = 0.608V * (1 + 6.98K/10K) = 1.033V$
 Frequency = 500 KHz
 OCP : 12.5A
 MAX system loading : 8.148A

	0.7
--	-----

(1) The device transitions into FCCM after the PGOOD pin goes high.

SS=1.4ms
Slew rate=3.3V/1.4ms = 2.35V/1ms
The slew rate of ramp up does not be over 20V/1ms.

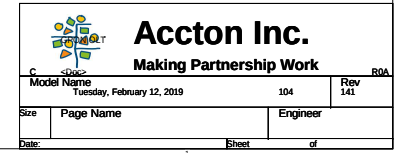
	0.7
--	-----

(1) The device transitions into FCCM after the PGOOD pin goes high.

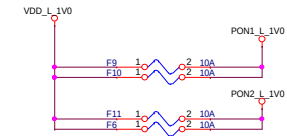
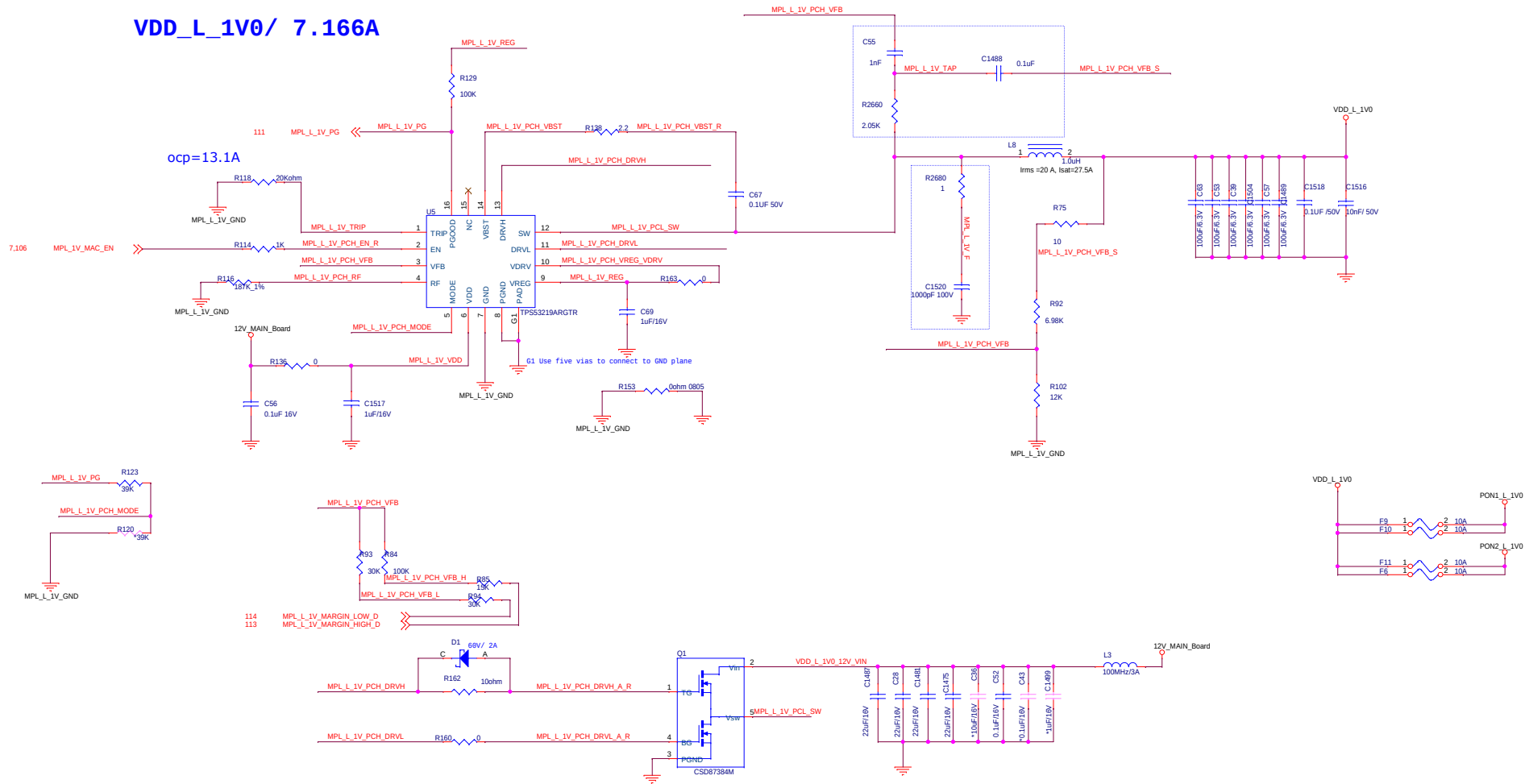
SS=1.4ms
Slew rate=3.3V/1.4ms = 2.35V/1ms
The slew rate of ramp up does not be over 20V/1ms.

12V to 1V
 $V_o = 0.608V * (1 + 6.98K/10K) = 1.033V$
 Frequency = 500 KHz
 OCP : 12.5A
 MAX system loading : 8.148A

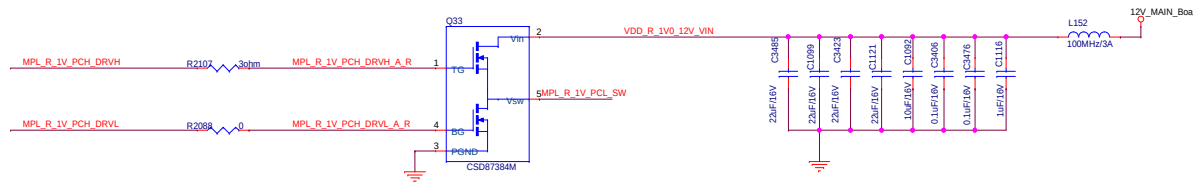
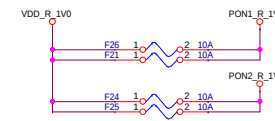
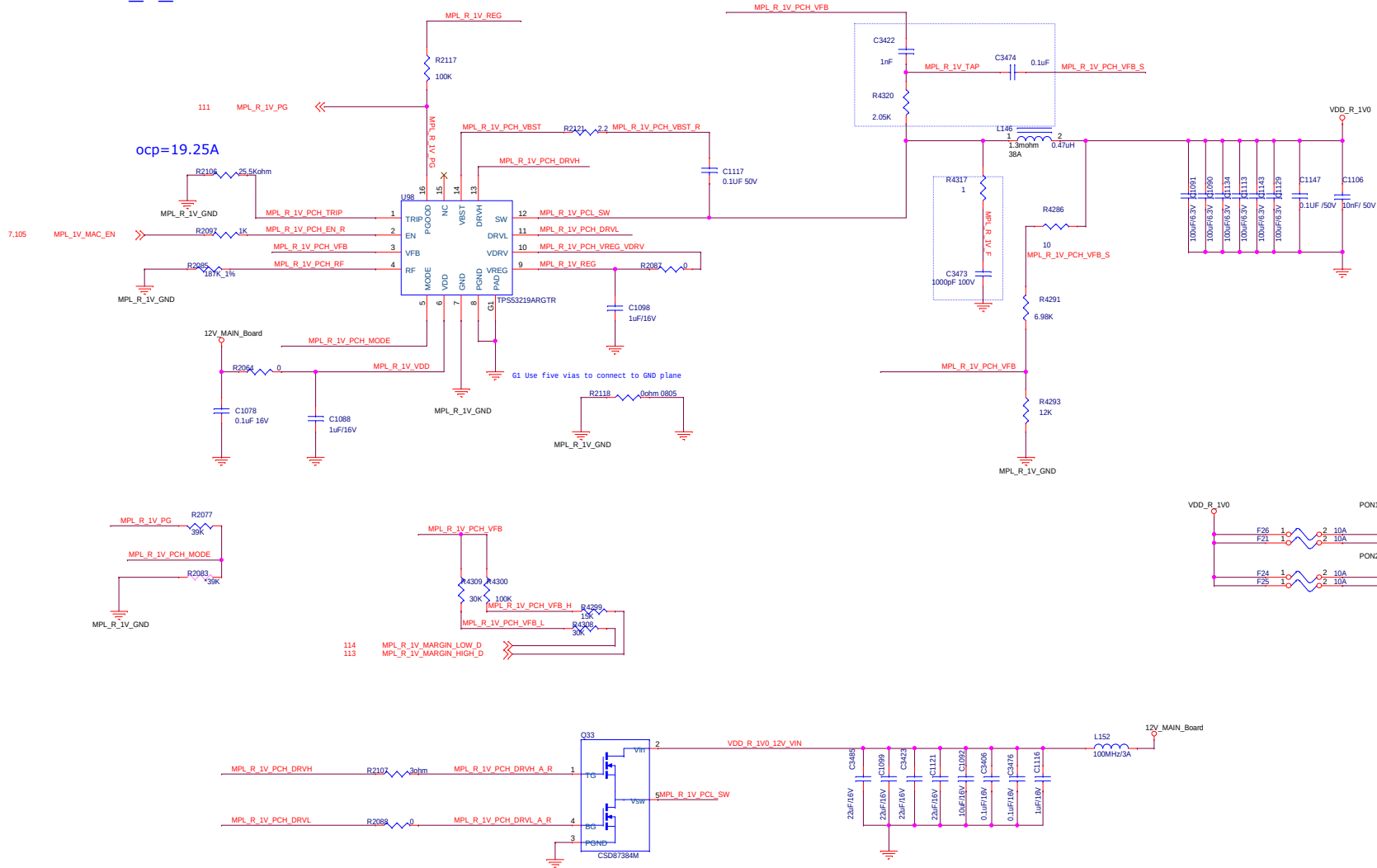
12V to 1V
 $V_o = 0.608V * (1 + 6.98K/10K) = 1.033V$
 Frequency = 500 KHz
 OCP : 12.5A
 MAX system loading : 8.148A

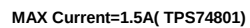
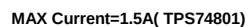


VDD_L_1V0/ 7.166A

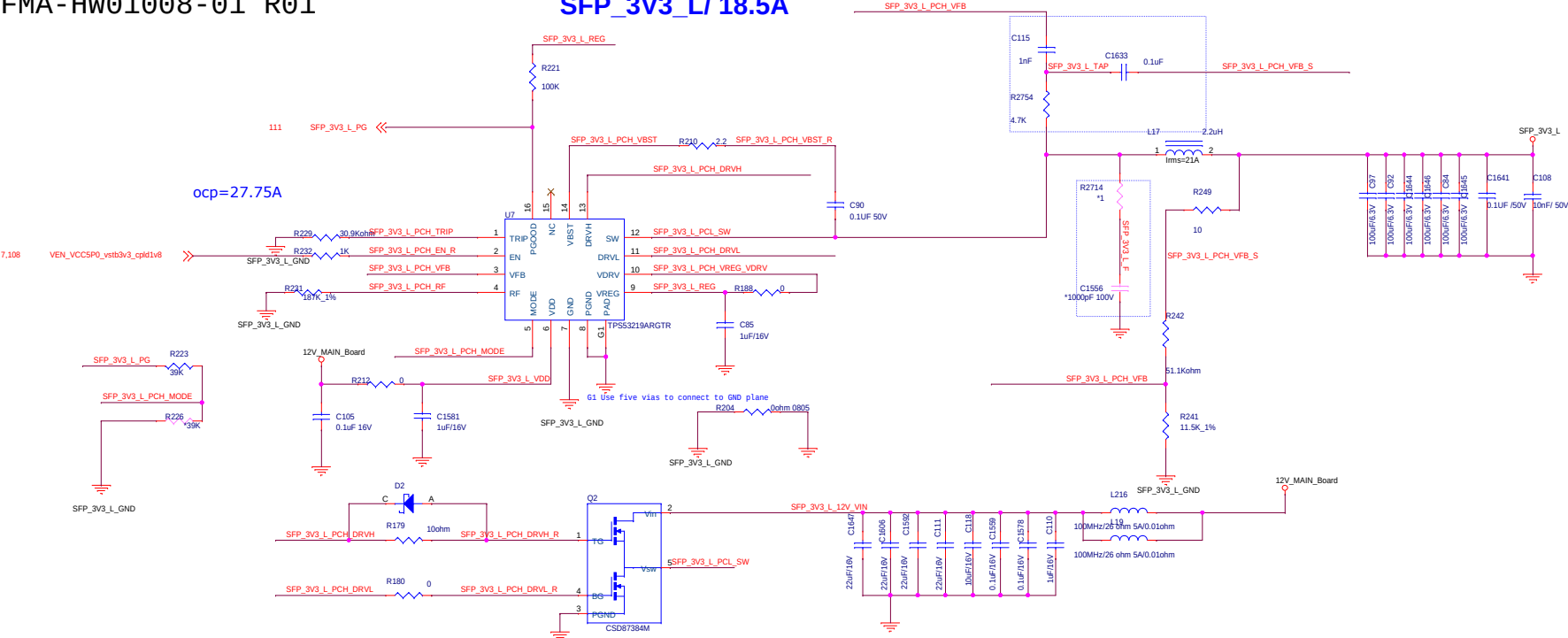


VDD_R_1V0/ 12.835A

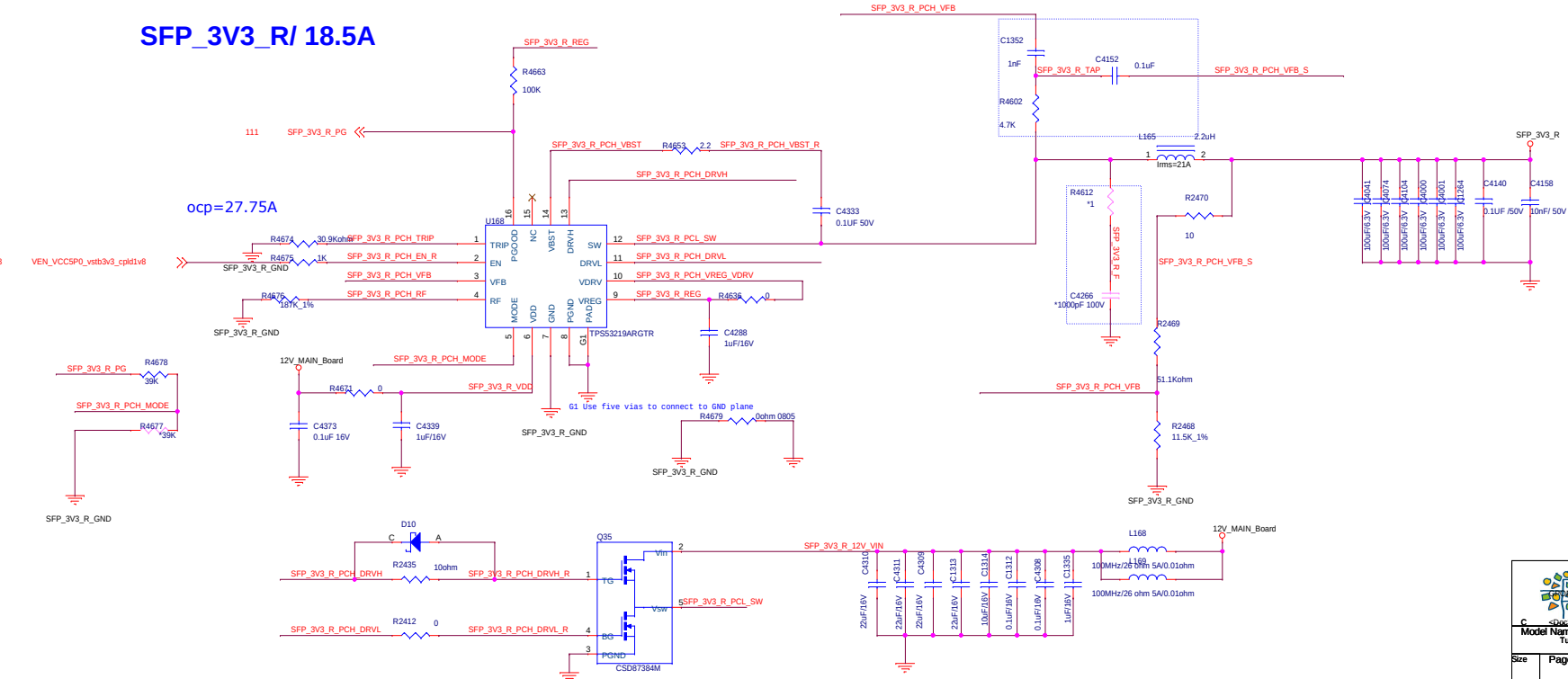




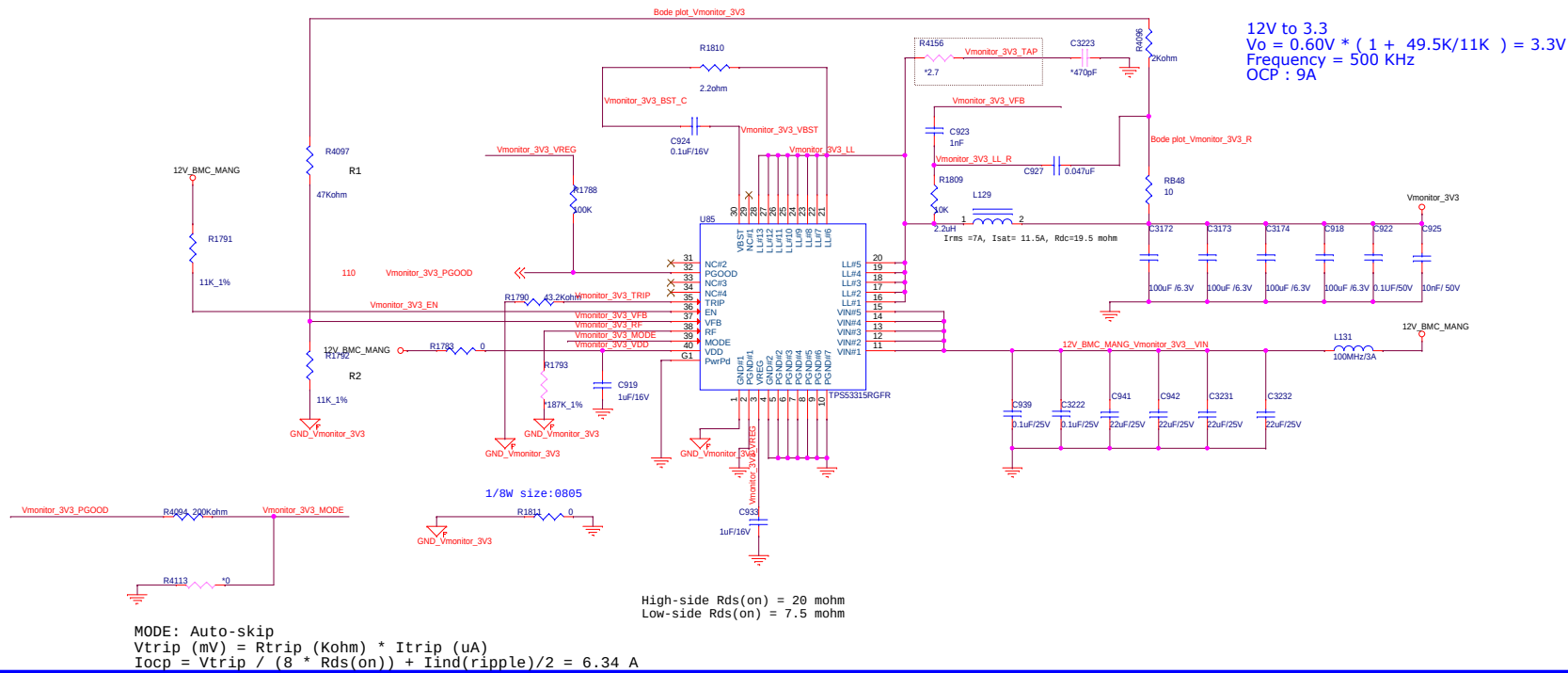
SFP_3V3_L/ 18.5A



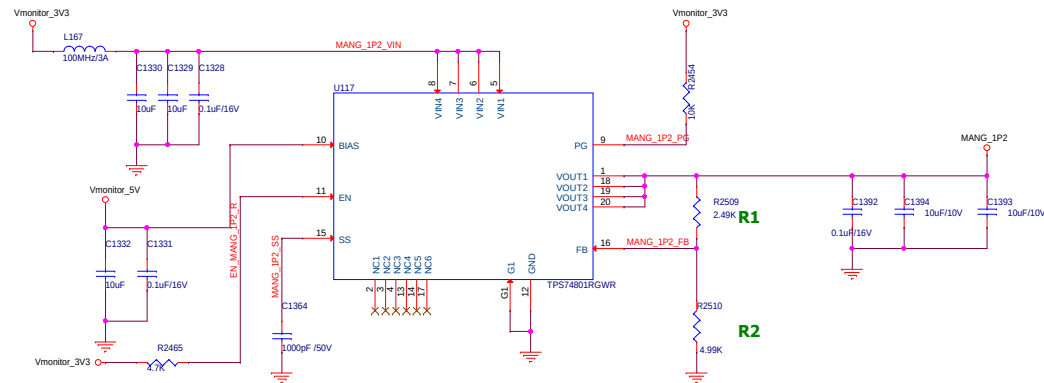
SFP_3V3_R/ 18.5A



Vmonitor_3V3/ 6.05A

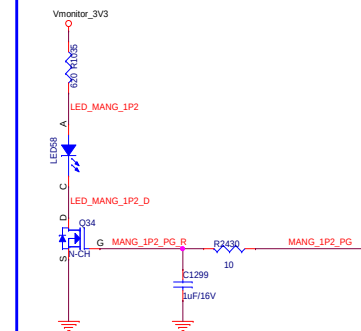


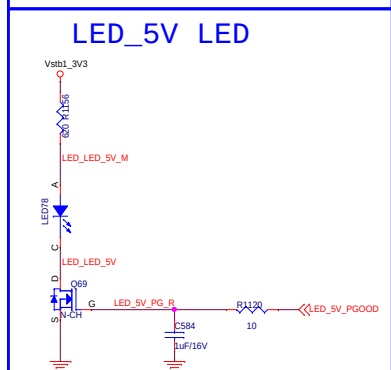
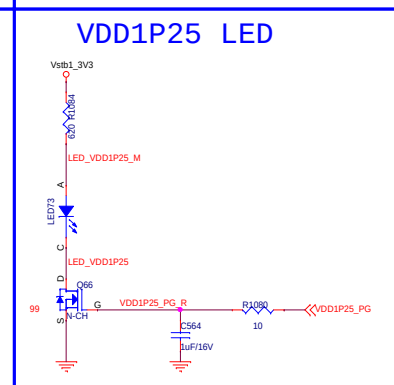
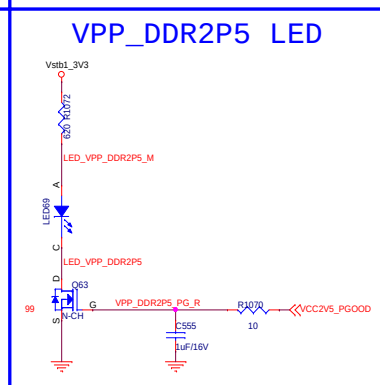
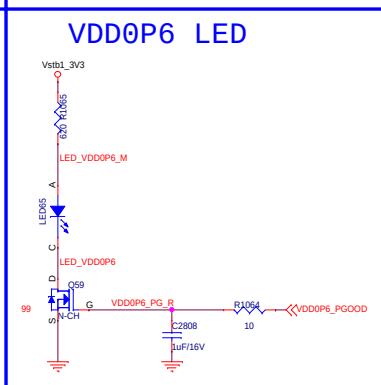
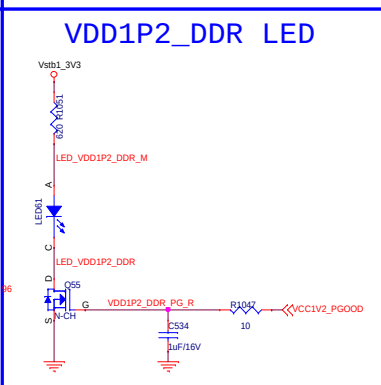
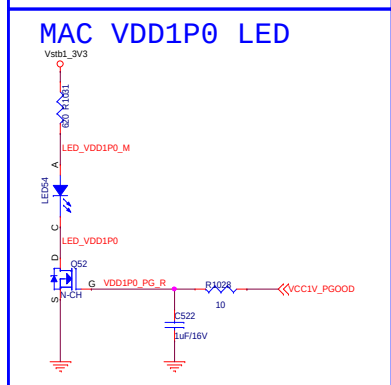
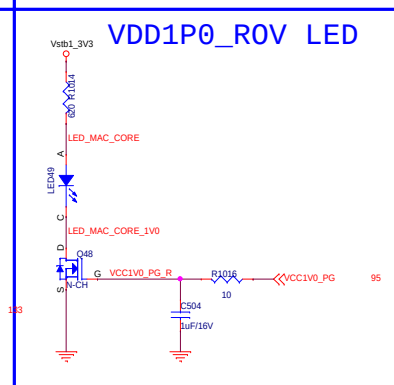
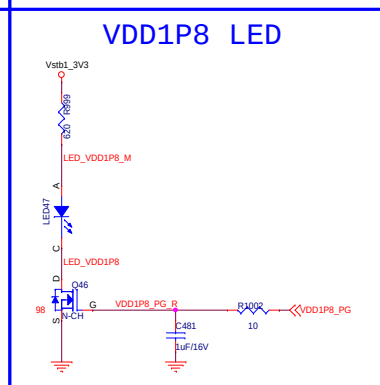
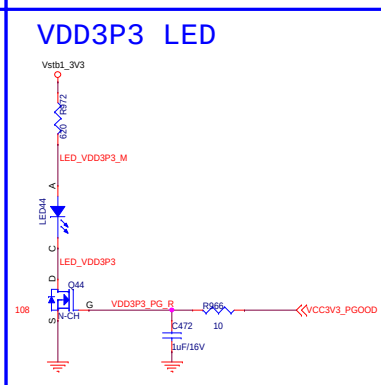
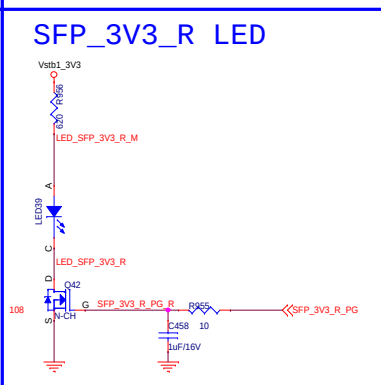
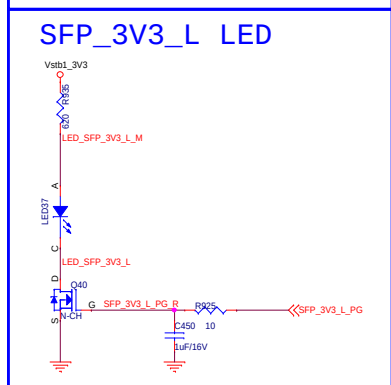
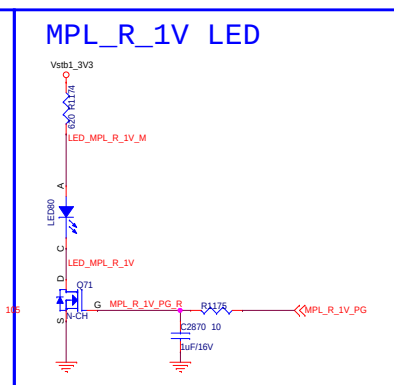
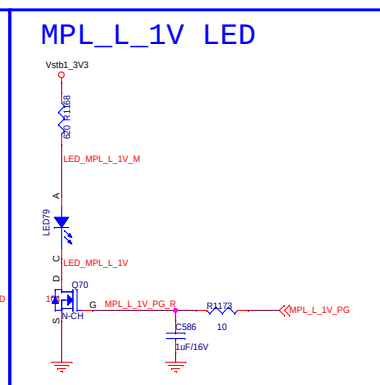
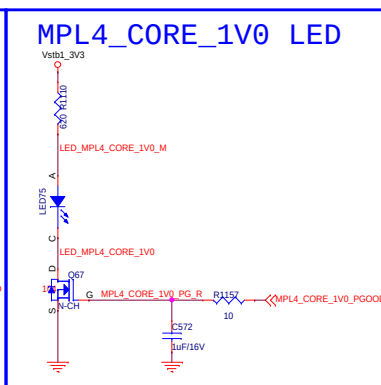
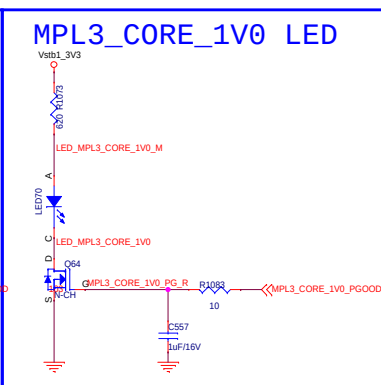
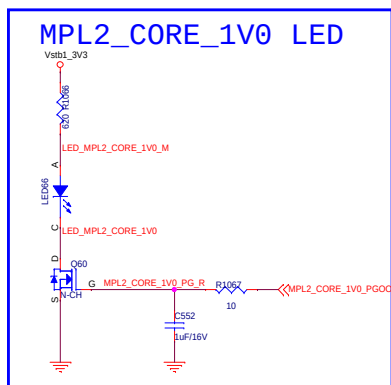
MANG_1P2/ 0.347A



MAX Current=1.5A(TPS74801)

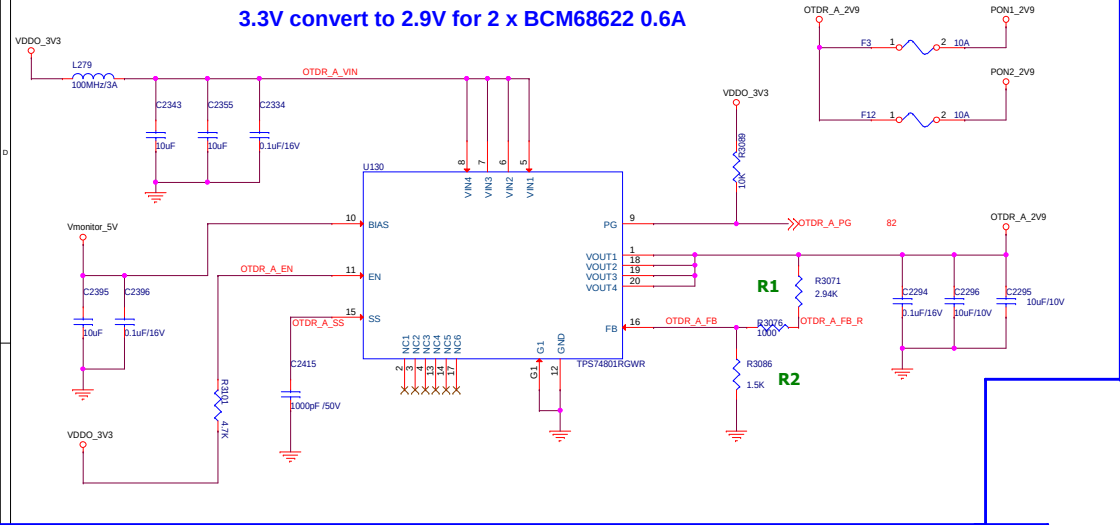
MANG PHY 1V2 LED



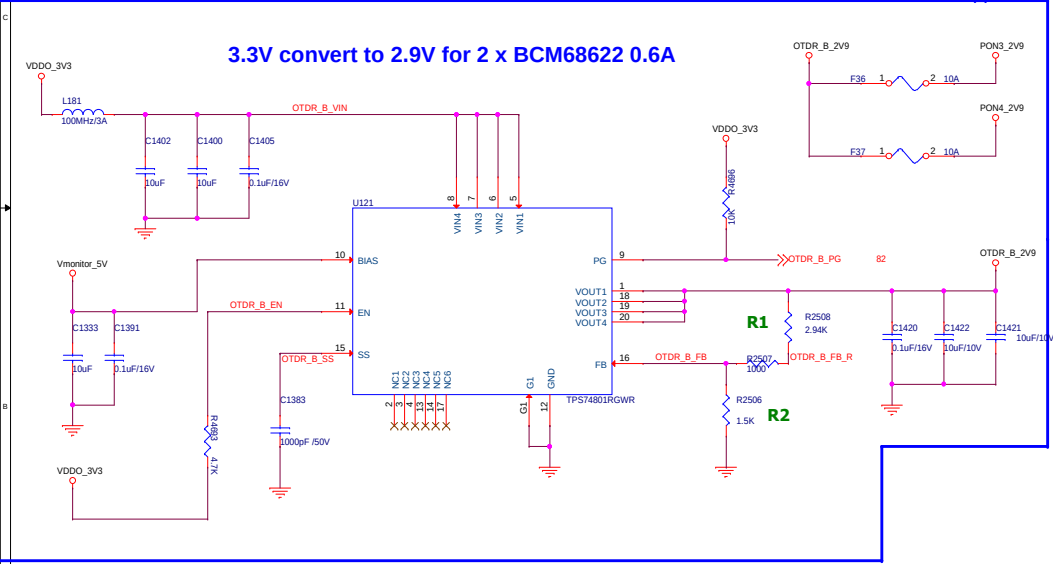


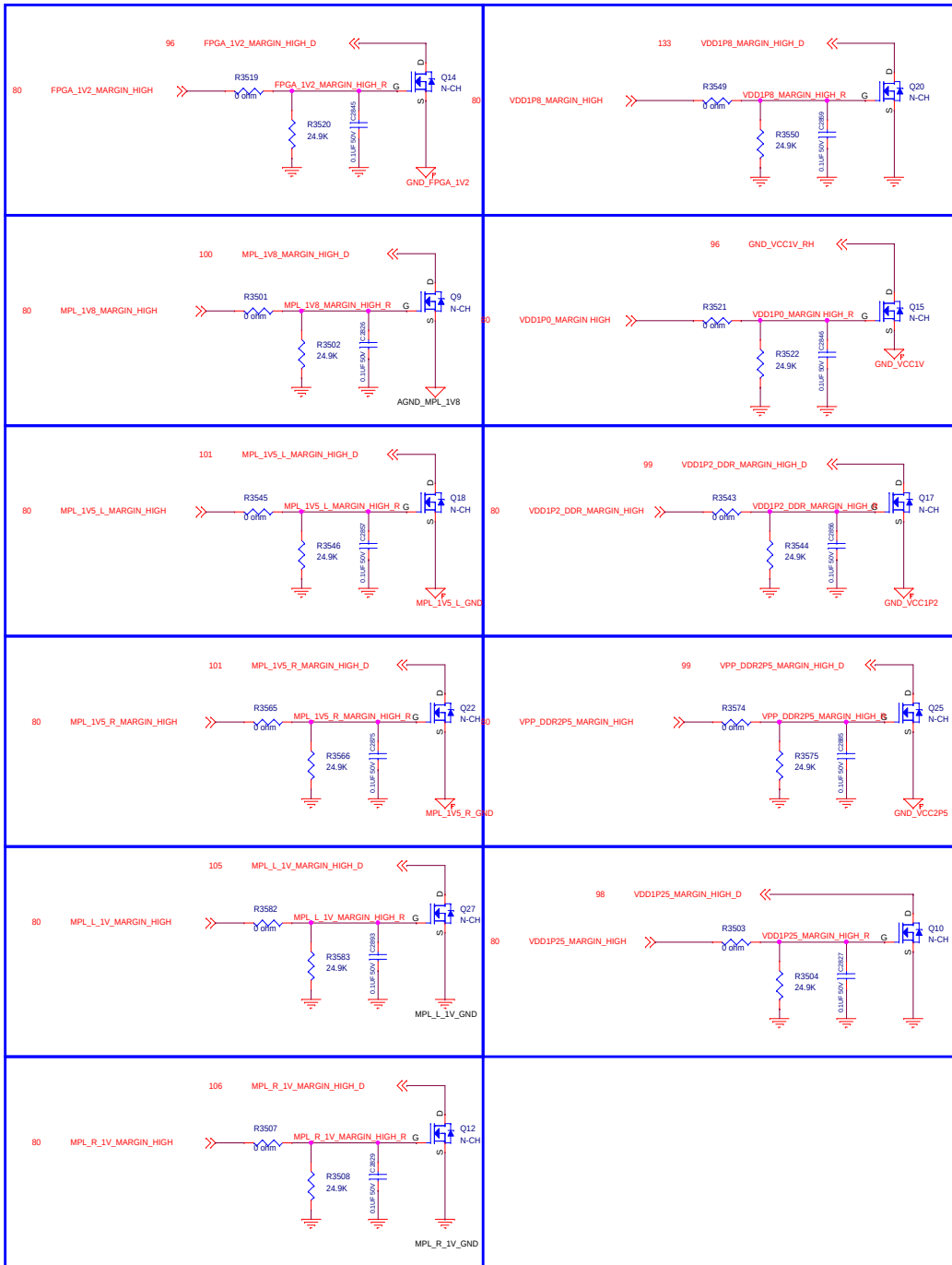
FMA-HW01008-01 R01

3.3V convert to 2.9V for 2 x BCM68622 0.6A

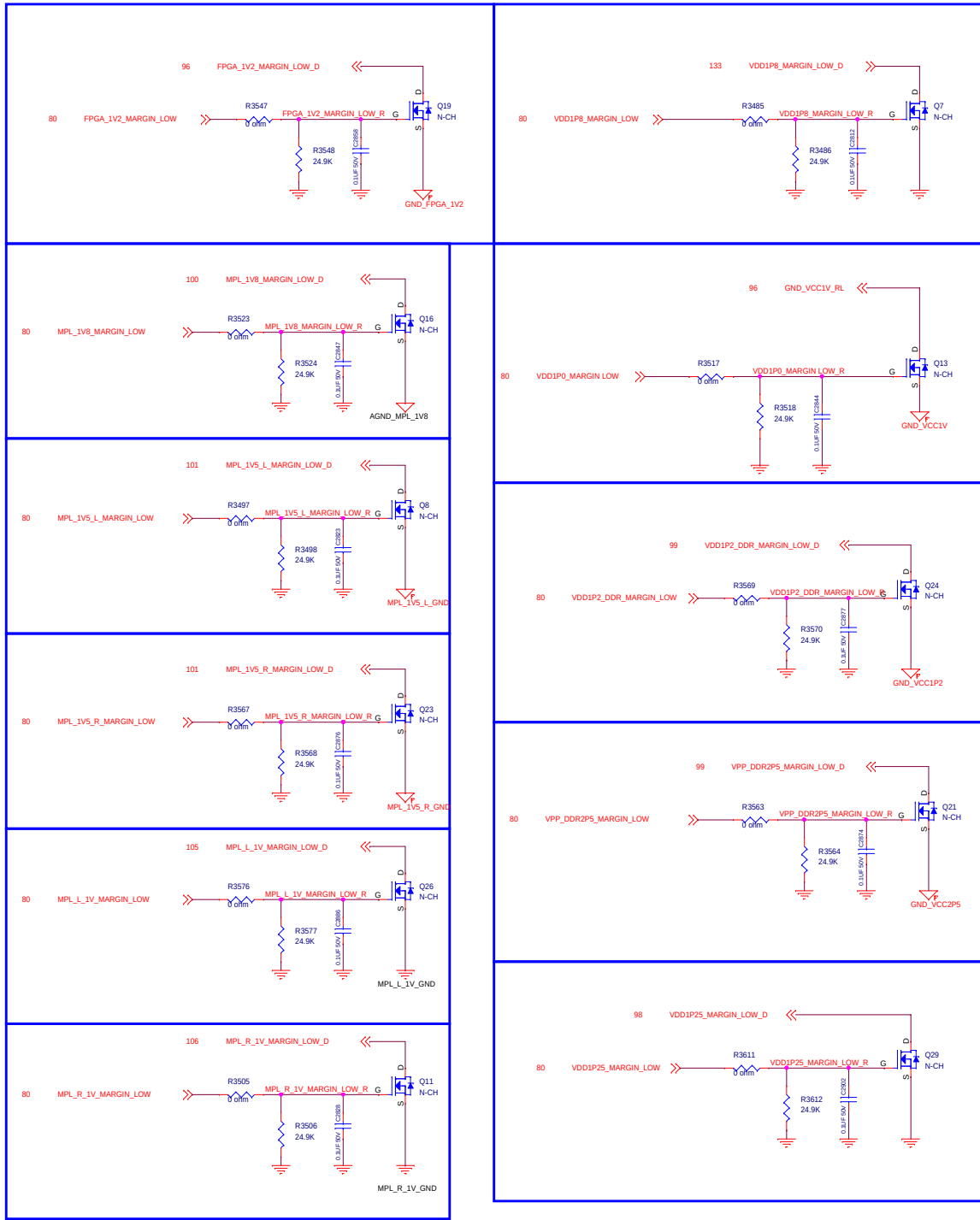


3.3V convert to 2.9V for 2 x BCM68622 0.6A





Margin High
(Margin High on)
(Margin Low on)
Margin Low
(Margin High off)
(Margin Low off)
Normal
(Margin High off)
(Margin Low on)

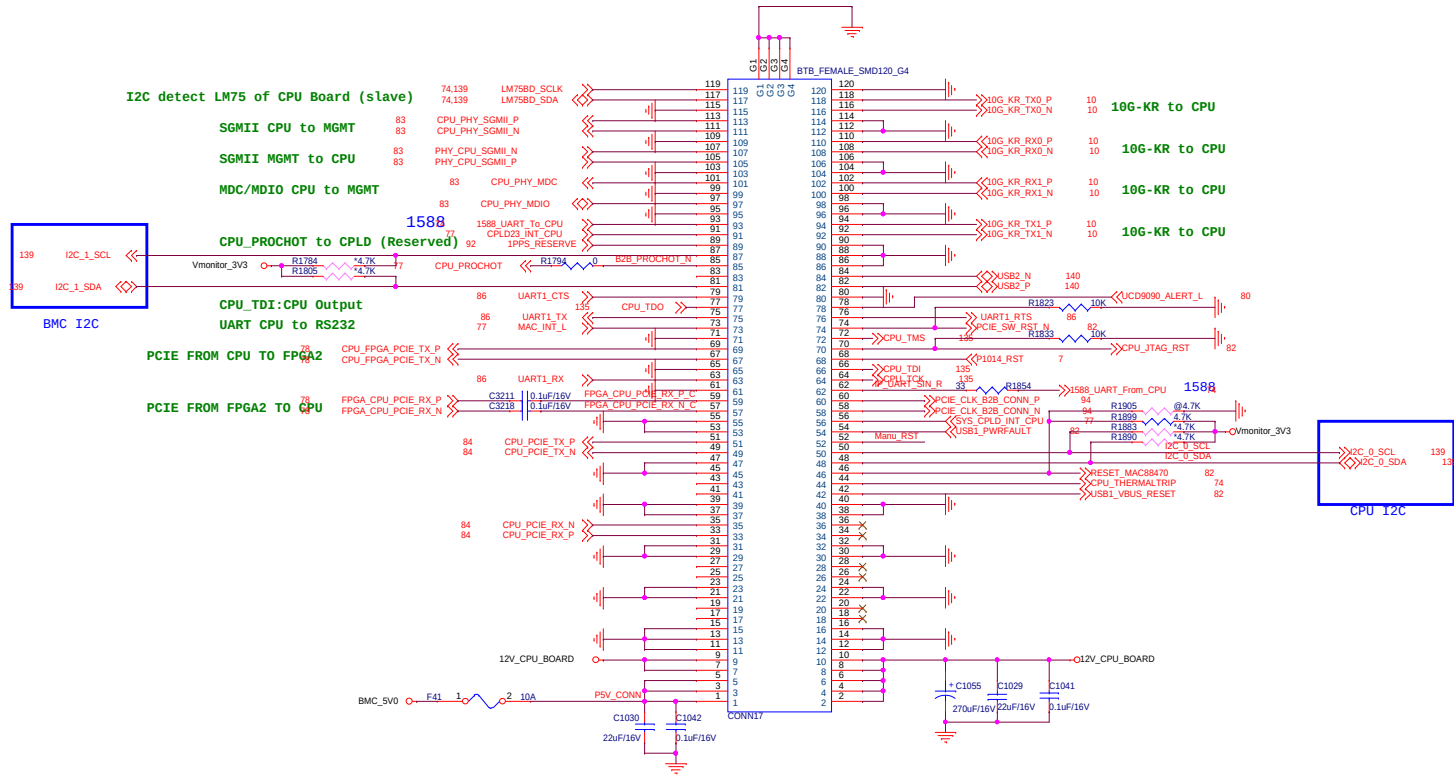


Margin High
(Margin High on)
(Margin Low on)
Margin Low
(Margin High off)
(Margin Low off)
Normal
(Margin High off)
(Margin Low on)



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115100000341A

Color	Forward Voltage	
O	2.4V	520ohm
G	3.8V	220ohm
B	3.8V	220ohm

QSFP28 Port_0



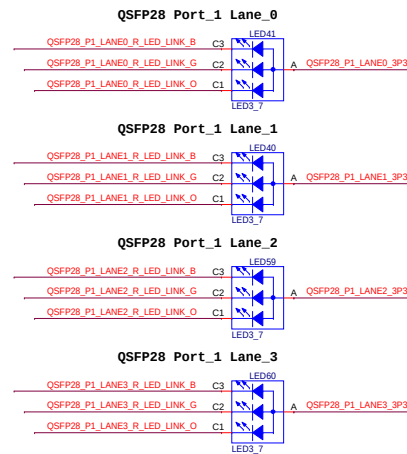
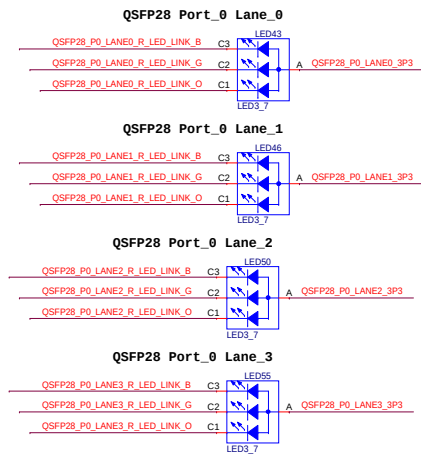
QSFP28 Port_1



115100000380A (mixer color)

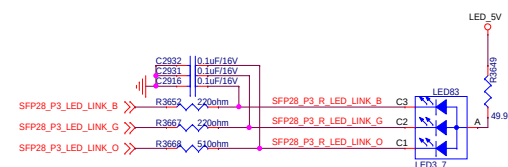
Color	Forward Voltage	
O->R	1.5V-2.15V	510ohm
G	2V-3.2V	220ohm
B	2V-3.2V	220ohm

R+G = 0

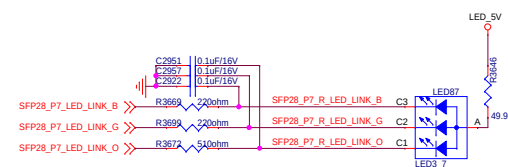


Color	Forward Voltage	
0	2.4V	520ohm
G	3.9V	220ohm
B	3.9V	

SFP28 Port_3

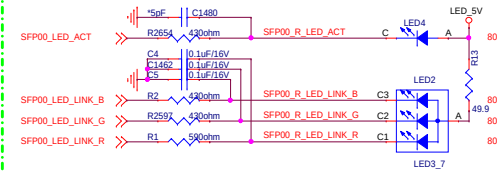


SFP28 Port_7

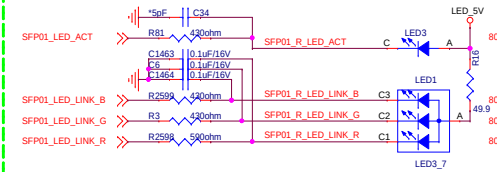


115100000085A
Color Forward Voltage
G 2.1V
1151000000238A
Color Forward Voltage
R 2.0V
G 3.0V
B 3.0V

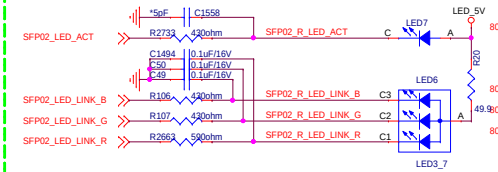
SFP Port_00



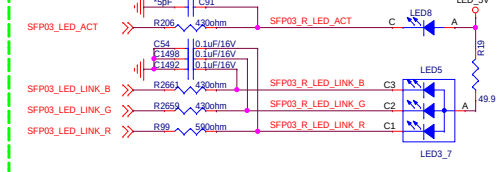
SFP Port_01



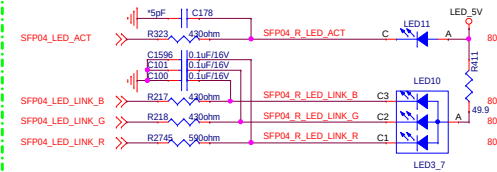
SFP Port_02



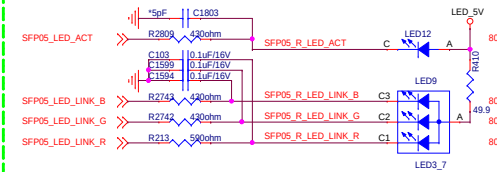
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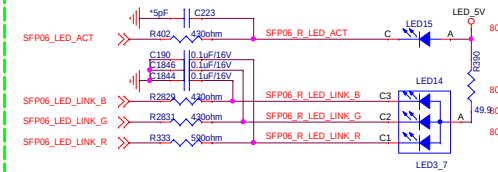
SFP Port_04



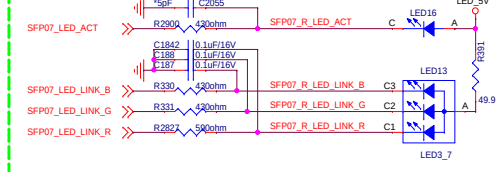
SFP Port_05



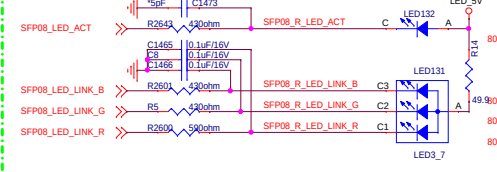
SFP Port_06



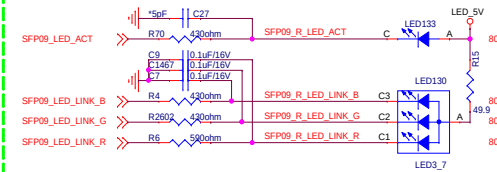
SFP Port_07



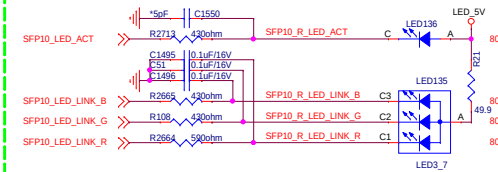
SFP Port_08



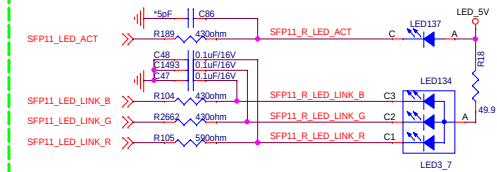
SFP Port_09



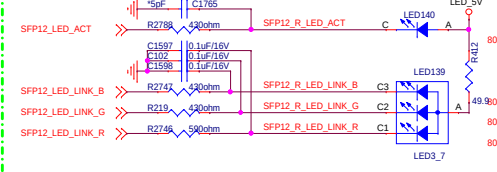
SFP Port_10



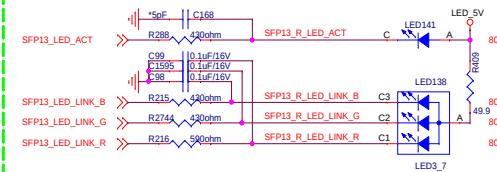
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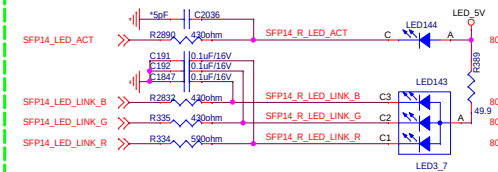
SFP Port_12



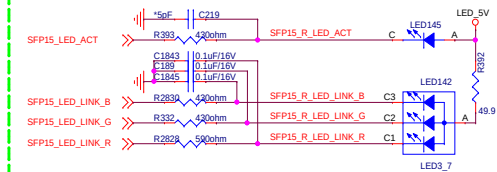
SFP Port_13



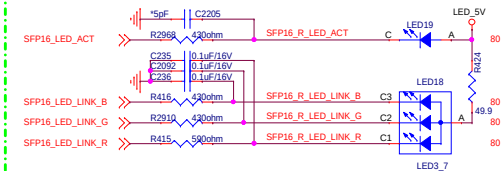
SFP Port_14



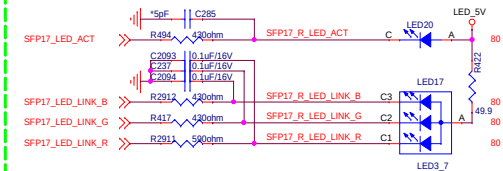
SFP Port_15



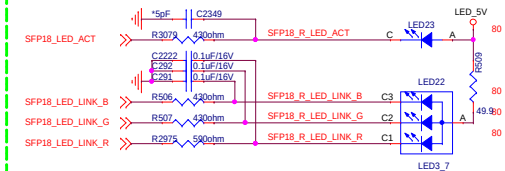
SFP Port_16



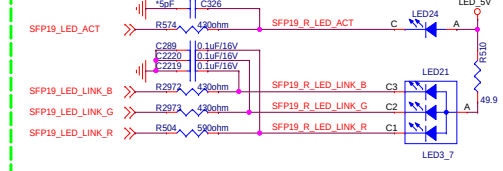
SFP Port_17



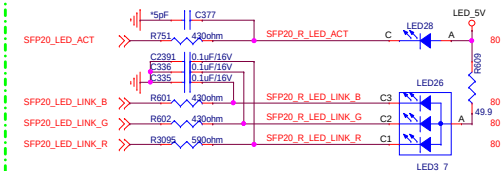
SFP Port_18



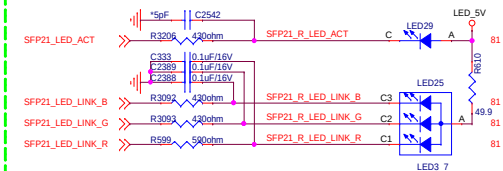
SFP Port_19



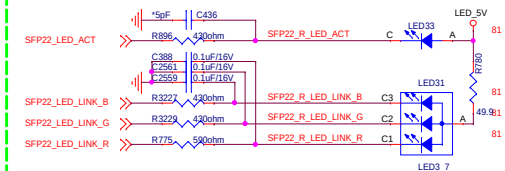
SFP Port_20



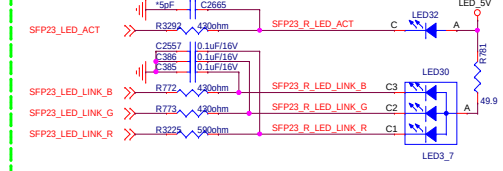
SFP Port_21



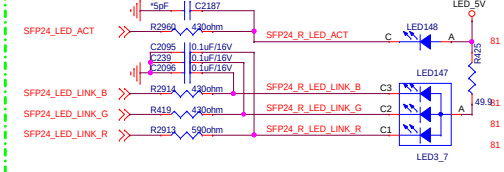
SFP Port_22



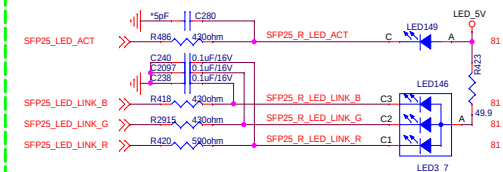
SFP Port_23



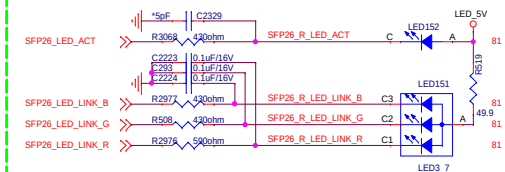
SFP Port_24



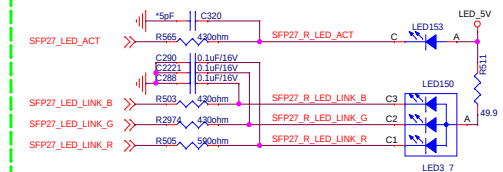
SFP Port_25



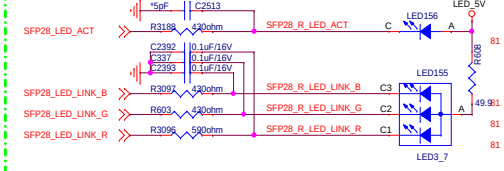
SFP Port_26



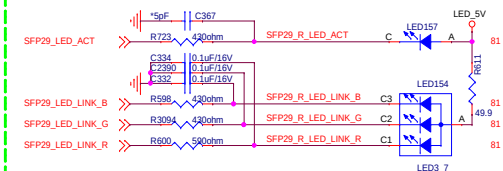
SFP Port_27



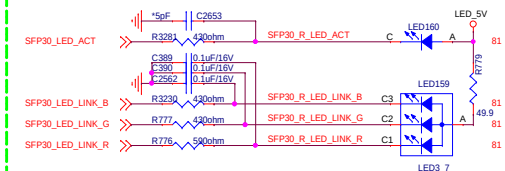
SFP Port_28



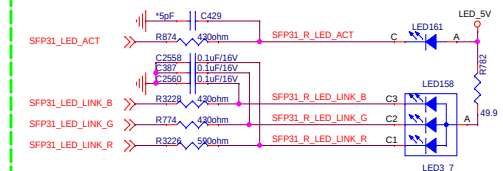
SFP Port_29



SFP Port_30



SFP Port_31

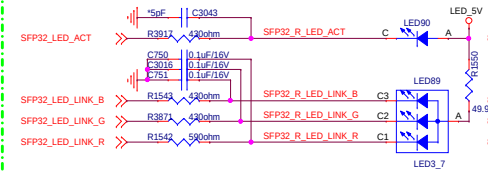


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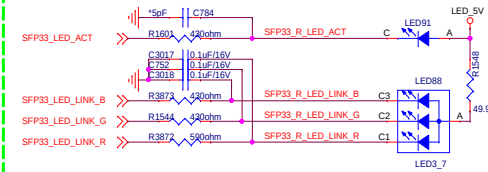
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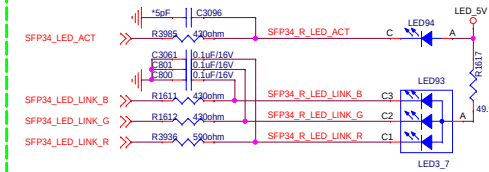
SFP Port_32



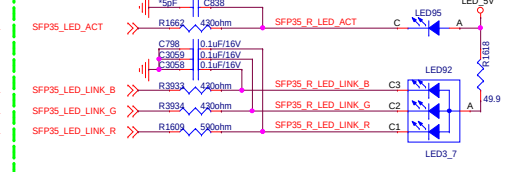
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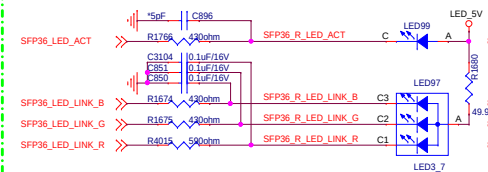
SFP Port_34



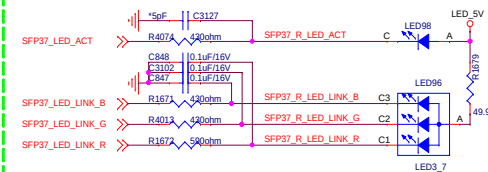
SFP Port_35



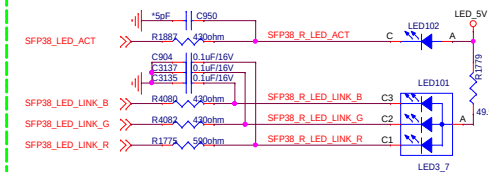
SFP Port_36



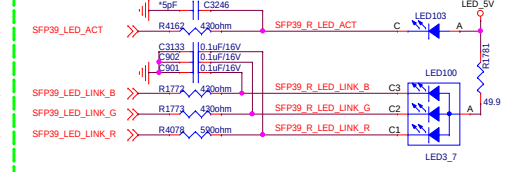
SFP Port_37



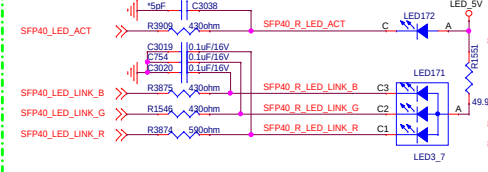
SFP Port_38



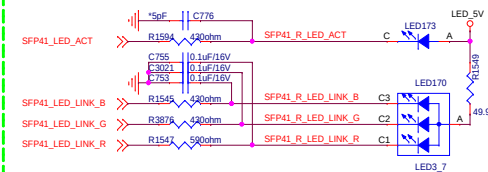
SFP Port_39



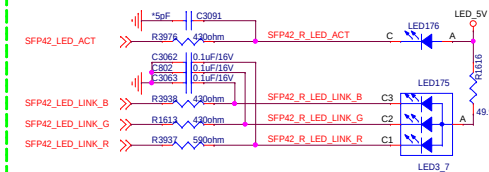
SFP Port_40



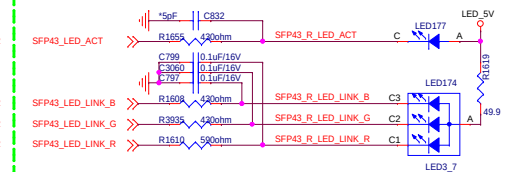
SFP Port_41



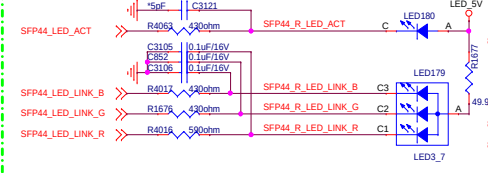
SFP Port_42



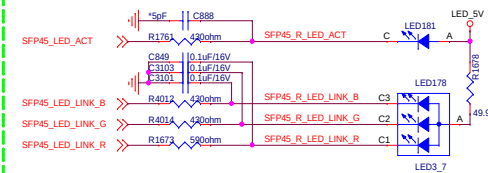
SFP Port_43



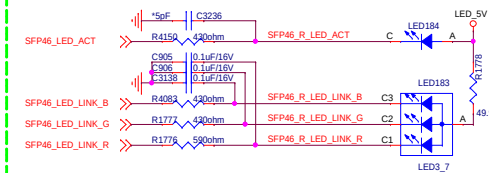
SFP Port_44



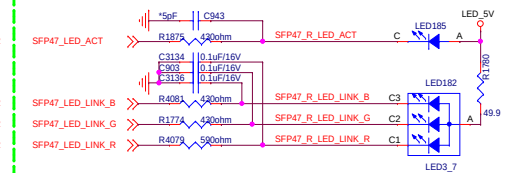
SFP Port_45



SFP Port_46



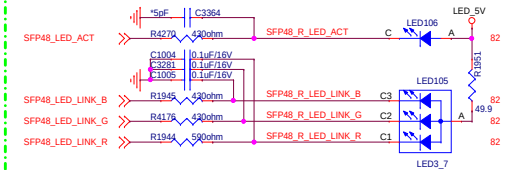
SFP Port_47



SFP Port_48

The schematic diagram for SFP Port_48 shows the following components and connections:

- Input Signals:**
 - SFP48_LED_ACT:** Connected to a 15pF capacitor, a 100ohm resistor (R427), and a 100ohm resistor (R428).
 - SFP48_LED_LINK_B:** Connected to a 100ohm resistor (R194F) and a 100ohm resistor (R194E).
 - SFP48_LED_LINK_G:** Connected to a 100ohm resistor (R417F) and a 100ohm resistor (R417E).
 - SFP48_LED_LINK_R:** Connected to a 100ohm resistor (R194F) and a 100ohm resistor (R194E).
- Output Signals:**
 - SFP48_R_LED_ACT:** Connected to a 100ohm resistor (R427) and a 100ohm resistor (R428).
 - SFP48_R_LED_LINK_B:** Connected to a 100ohm resistor (R194F) and a 100ohm resistor (R194E).
 - SFP48_R_LED_LINK_G:** Connected to a 100ohm resistor (R417F) and a 100ohm resistor (R417E).
 - SFP48_R_LED_LINK_R:** Connected to a 100ohm resistor (R194F) and a 100ohm resistor (R194E).
- LEDs:**
 - LED106:** Connected to SFP48_R_LED_ACT and SFP48_R_LED_LINK_B.
 - LED105:** Connected to SFP48_R_LED_LINK_G and SFP48_R_LED_LINK_R.
- Resistors:**
 - R427, R428:** 100ohm resistors.
 - R194F, R194E:** 100ohm resistors.
 - R417F, R417E:** 100ohm resistors.
- Capacitors:**
 - C3364:** 15pF capacitor.
 - C1004, C3261, C1005:** 0.1uF/16V capacitors.
- Other Components:**
 - LED3_7:** A 49.9 ohm resistor connected to the LED105 output.

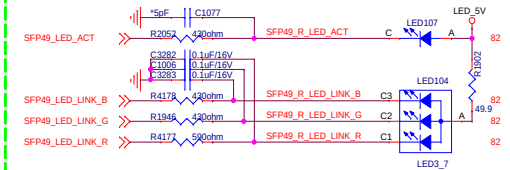


SFP Port_49

The diagram illustrates the internal circuitry of SFP Port_49. It features several signal traces on the left, each connected to a specific component on the right:

- SFP49_LED_ACT**: Connected to a 5pF capacitor (C1077) in series with a 400ohm resistor (R205). The signal then passes through a 400ohm resistor (R417A) and a 400ohm resistor (R194A) before reaching the LED107 and LED104 respectively.
- SFP49_LED_LINK_B**: Connected to a 10.1uF/16V capacitor (C3282) in series with a 400ohm resistor (R417B). The signal then passes through a 400ohm resistor (R194B) and a 400ohm resistor (R417) before reaching the LED107 and LED104 respectively.
- SFP49_LED_LINK_G**: Connected to a 10.1uF/16V capacitor (C3283) in series with a 400ohm resistor (R194A). The signal then passes through a 400ohm resistor (R417) and a 400ohm resistor (R194B) before reaching the LED107 and LED104 respectively.
- SFP49_LED_LINK_R**: Connected to a 10.1uF/16V capacitor (C3283) in series with a 400ohm resistor (R417). The signal then passes through a 400ohm resistor (R194B) and a 400ohm resistor (R417A) before reaching the LED107 and LED104 respectively.

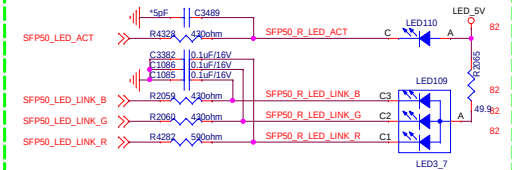
The output signals are connected to the LED107 and LED104, which are both connected to a common ground (LED3_7) and a 5V supply (LED+5V). The LED107 is connected to the LED+5V supply, and the LED104 is connected to the LED3_7 ground.



SFP Port_50

The diagram illustrates the internal circuitry of SFP Port_50. It features several signal traces and components:

- Input Signals:**
 - SFP50_LED_ACT:** Connected to a 50pF capacitor (C3489) and a 420ohm resistor (R432a), leading to the SFP50_R_LED_ACT signal.
 - SFP50_LED_LINK_B:** Connected to a 420ohm resistor (R205a), leading to the SFP50_R_LED_LINK_B signal.
 - SFP50_LED_LINK_G:** Connected to a 420ohm resistor (R205b), leading to the SFP50_R_LED_LINK_G signal.
 - SFP50_LED_LINK_R:** Connected to a 500ohm resistor (R428a), leading to the SFP50_R_LED_LINK_R signal.
- Output Signals:**
 - SFP50_R_LED_ACT:** Connected to an LED110 through a 20k5 resistor (R2045) to LED 5V.
 - SFP50_R_LED_LINK_B, SFP50_R_LED_LINK_G, SFP50_R_LED_LINK_R:** These signals are connected to a multi-pin connector (LED109) through capacitors C3, C2, and C1 respectively. The connector is also connected to LED0_7.
- Capacitors:**
 - C3489: 50pF
 - C108b: 0.1uF/16V
 - C108c: 0.1uF/16V
 - C3: 0.1uF/16V
 - C2: 0.1uF/16V
 - C1: 0.1uF/16V
- Resistors:**
 - R432a: 420ohm
 - R205a: 420ohm
 - R205b: 420ohm
 - R428a: 500ohm
 - R2045: 20k5
- LEDs:**
 - LED110: Connected to SFP50_R_LED_ACT and LED 5V.
 - LED109: A multi-pin connector connected to SFP50_R_LED_LINK_B, SFP50_R_LED_LINK_G, SFP50_R_LED_LINK_R, and LED0_7.

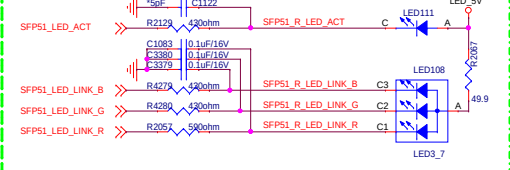


SFP Port_51

The diagram illustrates the electrical connections for the SFP Port_51. It shows four signal lines originating from the left and connecting to LEDs on the right. The components and their values are as follows:

- SFPS1_LED_ACT:** Connected to LED111. The signal path includes a 50pF capacitor (C1122) and a 120ohm resistor (R2129). The LED is labeled LED111 and has a 5V supply and a 200V rating.
- SFPS1_LED_LINK_B:** Connected to LED108. The signal path includes a 10 1uF/16V capacitor (C1083), a 0.1uF/16V capacitor (F1380), a 0.1uF/16V capacitor (C1082), and a 120ohm resistor (R4279). The LED is labeled LED108 and has a 49.9V supply.
- SFPS1_LED_LINK_G:** Connected to LED3_7. The signal path includes a 120ohm resistor (R4286).
- SFPS1_LED_LINK_R:** Connected to LED3_7. The signal path includes a 500ohm resistor (R2051).

The LEDs are labeled LED111, LED108, and LED3_7. The supply voltages are 5V and 49.9V. The resistors are labeled R2129, R4279, R4286, and R2051. The capacitors are labeled C1122, C1083, F1380, C1082, and C1081.



SFP Port_52

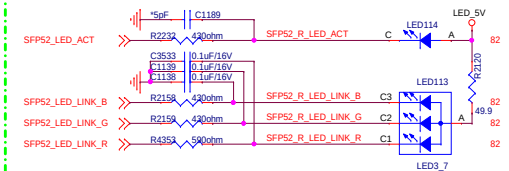
The diagram illustrates the internal circuitry of SFP Port_52. It features several signal traces on the left, each with a termination resistor and a bypass capacitor to ground:

- SFP52_LED_ACT**: Connected to a 50pF capacitor (C1189) and a 400ohm resistor (R2234).
- SFP52_LED_LINK_B**: Connected to a 50pF capacitor (C1190) and a 400ohm resistor (R2158).
- SFP52_LED_LINK_G**: Connected to a 50pF capacitor (C1191) and a 400ohm resistor (R2159).
- SFP52_LED_LINK_R**: Connected to a 50pF capacitor (C1192) and a 400ohm resistor (R4353).

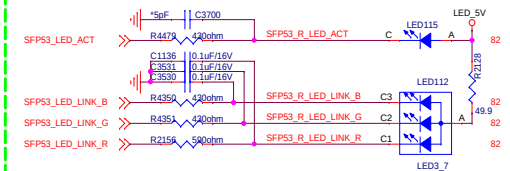
These traces connect to various components on the right:

- SFP52_R_LED_ACT**: A signal trace that connects to the cathode of LED114.
- SFP52_R_LED_LINK_B**: A signal trace that connects to the cathode of LED113.
- SFP52_R_LED_LINK_G**: A signal trace that connects to the cathode of LED113.
- SFP52_R_LED_LINK_R**: A signal trace that connects to the cathode of LED113.

LED114 is connected to a 5V supply (LED+5V) through a 220ohm resistor (R2120). LED113 is connected to a 5V supply (LED+5V) through a 49.9ohm resistor (R499). The diagram also shows a 500ohm resistor (R4354) connected to the SFP52_R_LED_LINK_R trace.



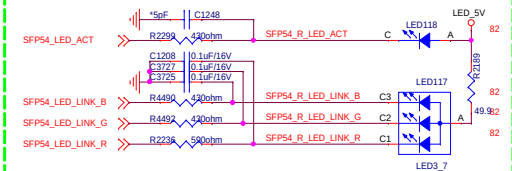
SFP Port_53



SFP Port_54

The diagram illustrates the internal circuitry of SFP Port_54. It features several signal traces and components:

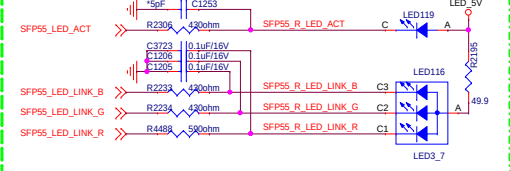
- LED Drivers:** Four LEDs (LED118, LED117, LED3_7) are connected to the port. Each LED is driven by a current source (R2259, R4459, R2238) and a capacitor (C1248, C1208, C3727, C3725). The LEDs are connected to a common LED SV supply and a common ground (49.92).
- Signal Traces:** The diagram shows traces for SFP54_LED_ACT, SFP54_LED_LINK_B, SFP54_LED_LINK_G, and SFP54_LED_LINK_R. These traces are connected to the corresponding LED drivers.
- Components:** The components are labeled with their values: R2259 (50F), C1248 (400nm), R1208 (10.1uF/16V), C3727 (0.1uF/16V), C3725 (0.1uF/16V), R4459 (400nm), R2238 (500nm), LED118, LED117, LED3_7, and 49.92.



SFP Port_55

The schematic diagram for SFP Port_55 shows the following components and connections:

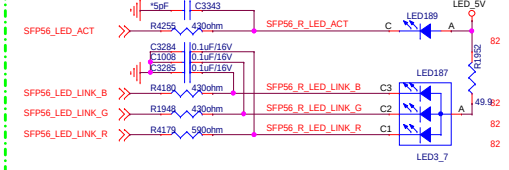
- Input Signals:**
 - SFP55_LED_ACT
 - SFP55_LED_LINK_B
 - SFP55_LED_LINK_G
 - SFP55_LED_LINK_R
- Resistors:**
 - R2306 (120ohm) connected to SFP55_LED_ACT
 - R2233 (120ohm) connected to SFP55_LED_LINK_B
 - R2234 (120ohm) connected to SFP55_LED_LINK_G
 - R4488 (500ohm) connected to SFP55_LED_LINK_R
- Capacitors:**
 - *56F (56pF) and C1253 (10.1uF/15V) connected to SFP55_LED_ACT
 - C1252 (10.1uF/15V), C1256 (0.1uF/15V), and C1205 (0.1uF/15V) connected to SFP55_LED_LINK_B
- LEDs:**
 - LED119 connected to SFP55_LED_ACT
 - LED116 connected to SFP55_LED_LINK_B
 - LED3_7 connected to SFP55_LED_LINK_G and SFP55_LED_LINK_R
- Other Components:**
 - LED155 (49.9) connected to SFP55_LED_LINK_B



SFP Port_56

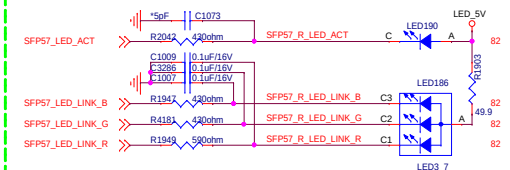
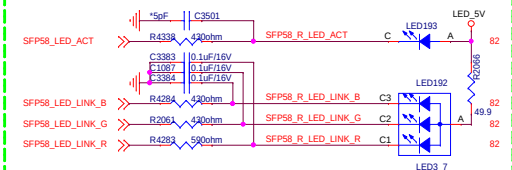
The schematic diagram for SFP Port_56 shows the following components and connections:

- Inputs:** SFP56_LED_ACT, SFP56_LED_LINK_B, SFP56_LED_LINK_G, and SFP56_LED_LINK_R.
- Resistors:**
 - R4255 (430ohm) connected to SFP56_LED_ACT.
 - R4180 (430ohm) connected to SFP56_LED_LINK_B.
 - R1948 (430ohm) connected to SFP56_LED_LINK_G.
 - R4179 (500ohm) connected to SFP56_LED_LINK_R.
- Capacitors:**
 - C3343 (50pF) connected to SFP56_LED_ACT.
 - C3284 (0.1uF/16V), C1008 (0.1uF/16V), and C3285 (0.1uF/16V) connected to SFP56_LED_LINK_B.
- LEDs:**
 - LED189 connected to SFP56_LED_ACT.
 - LED187 connected to SFP56_LED_LINK_B, SFP56_LED_LINK_G, and SFP56_LED_LINK_R.
- Other Labels:** LED_5V, C, A, B, C3, C2, C1, LED3_7, 82, 49, 82.



SFP Port_57

The diagram shows the internal wiring of SFP Port_57. On the left, five signal traces enter: SFP57_LED_ACT, SFP57_LED_LINK_B, SFP57_LED_LINK_G, and SFP57_LED_LINK_R. Each trace passes through a series of components: a capacitor (C1009, C1026, C1007, C1194, C1418, or C1949), a resistor (R2042, R1941, R1418, or R1949), and a 40ohm or 50ohm termination resistor. The traces then connect to various components on the right: SFP57_R_LED_ACT to LED190, SFP57_R_LED_LINK_B to C3, SFP57_R_LED_LINK_G to C2, SFP57_R_LED_LINK_R to C1, and LED186. A 5V LED supply is connected to the LED190 and LED186. The diagram also shows a 49.9k resistor connected to the LED186 and a LED3_7 component.

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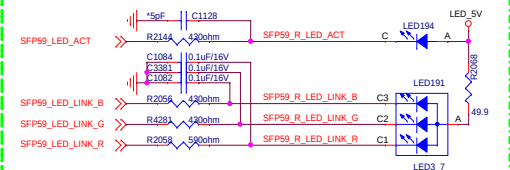
The schematic diagram illustrates the electrical connections for SFP Port_59. It features several signal traces on the left, each connected to a specific component on the right:

- SFP59_LED_ACT** is connected to a 5pF capacitor (C1128) in series with a 50ohm resistor (R214), which then connects to the SFP59_R_LED_ACT signal.
- SFP59_LED_LINK_B** is connected to a series combination of capacitors C381 (0.1uF/16V) and C1362 (0.1uF/16V), followed by a 50ohm resistor (R2056), leading to the SFP59_R_LED_LINK_B signal.
- SFP59_LED_LINK_G** is connected to a 50ohm resistor (R4281), leading to the SFP59_R_LED_LINK_R signal.
- SFP59_LED_LINK_R** is connected to a 50ohm resistor (R2059), leading to the SFP59_R_LED_LINK_R signal.

On the right side, the signals are connected to the SFP module's internal components:

- SFP59_R_LED_ACT** connects to LED194, which is powered by a 5V supply and has a 200ohm resistor (R2048) connected to its cathode.
- SFP59_R_LED_LINK_B** connects to input C3 of LED191.
- SFP59_R_LED_LINK_R** connects to input C1 of LED191.
- SFP59_R_LED_LINK_G** connects to input C2 of LED191.

LED191 is a 3-pin LED with a common anode (A) connected to a 49.9V supply.



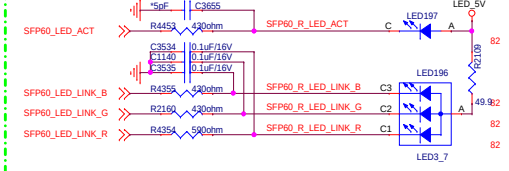
The diagram illustrates the internal circuitry of SFP Port_60. It features several signal traces on the left, each connected to a specific component:

- SFP60_LED_ACT**: Connected to a 5pF capacitor, an R4453 resistor (430ohm), and an LED197.
- SFP60_LED_LINK_B**: Connected to a 5pF capacitor, an R4355 resistor (430ohm), and an LED196.
- SFP60_LED_LINK_G**: Connected to an R2165 resistor (430ohm) and an LED196.
- SFP60_LED_LINK_R**: Connected to an R4354 resistor (430ohm) and an LED196.

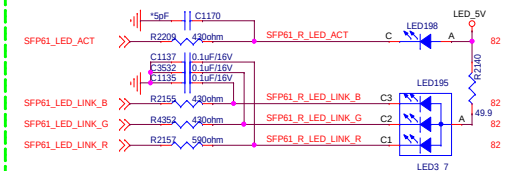
The components are labeled with their respective values and part numbers:

- Capacitors: 5pF
- Resistors: R4453 (430ohm), R4355 (430ohm), R2165 (430ohm), R4354 (430ohm)
- LEDs: LED197, LED196, LED3_7

The diagram also shows a 5V supply connected to the LED197 and LED196, and a 1.2V supply connected to the LED3_7.



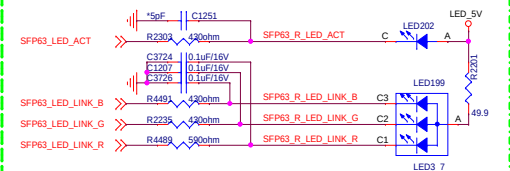
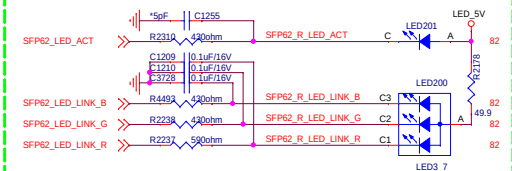
SFP Port_61



SFP Port_62

The schematic diagram for SFP Port_62 shows the following components and connections:

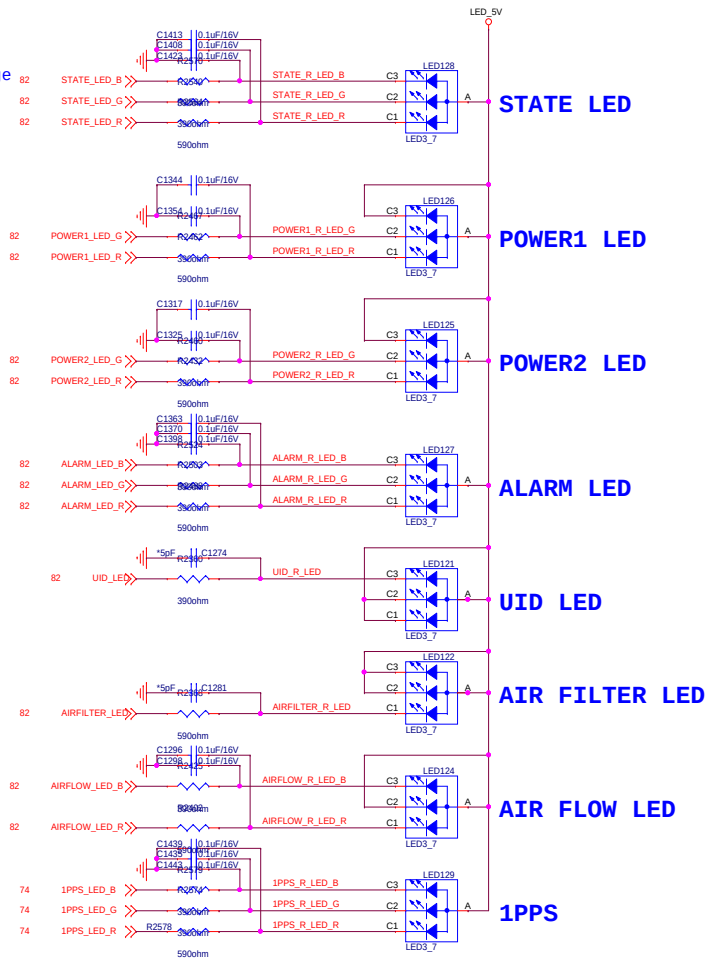
- LEDs:** LED201, LED200, and LED3_7.
- Resistors:** R231A (100ohm), R449A (100ohm), R238A (100ohm), and R223A (500ohm).
- Capacitors:** C1255 (10.1uF/16V), C1209 (10.1uF/16V), C1210 (10.1uF/16V), C3728 (10.1uF/16V), C3 (100nF), C2 (100nF), and C1 (100nF).
- Signal Traces:** SFP62_LED_ACT, SFP62_R_LED_ACT, SFP62_LED_LINK_B, SFP62_R_LED_LINK_B, SFP62_LED_LINK_G, SFP62_R_LED_LINK_G, SFP62_LED_LINK_R, and SFP62_R_LED_LINK_R.
- Power:** LED_5V and LED3_7.



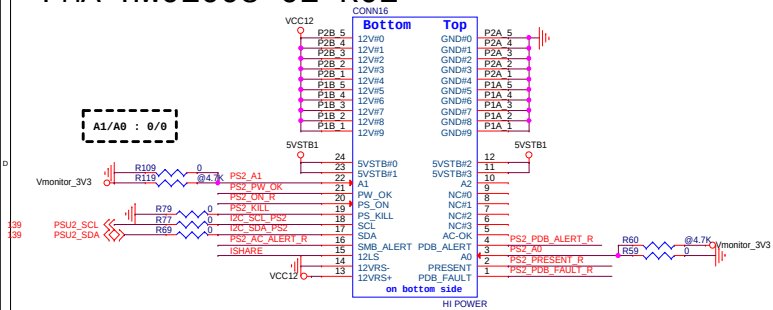
Making Partnership Work

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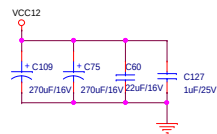
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B	3V



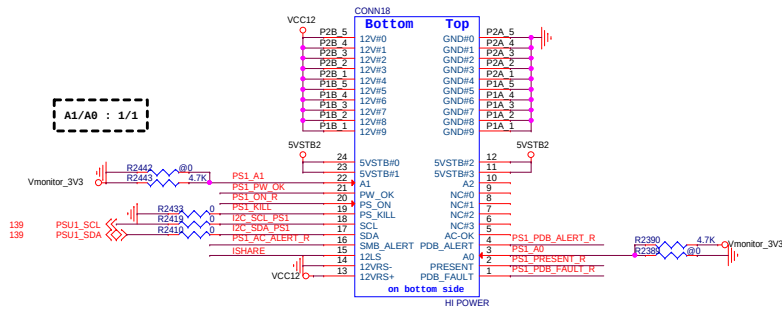
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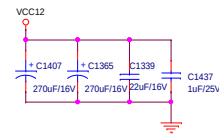
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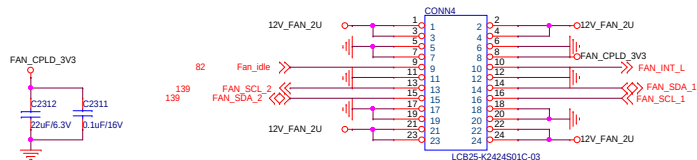
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PS 12V OK	1 : 12V output Good 0 : 12V output fail
PS ALERT	1 : OK 0 : Alert to system
PS Present	0 : Present 1 : Not present



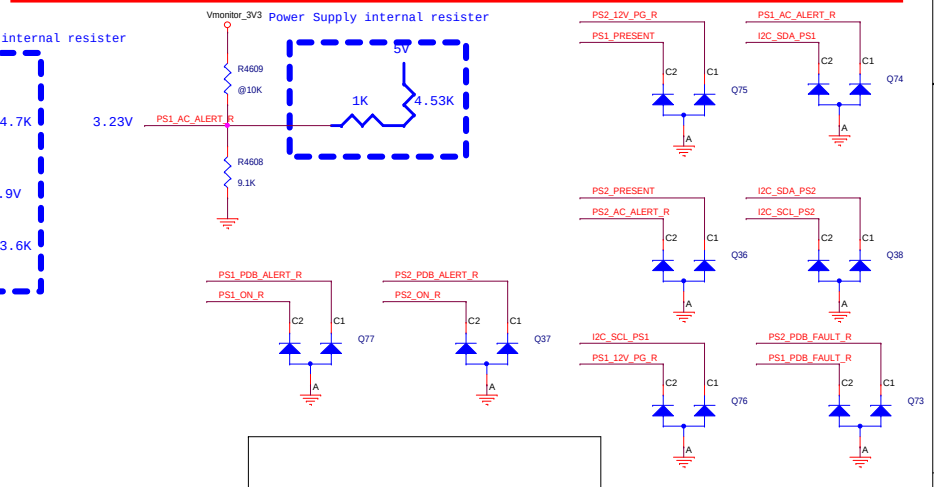
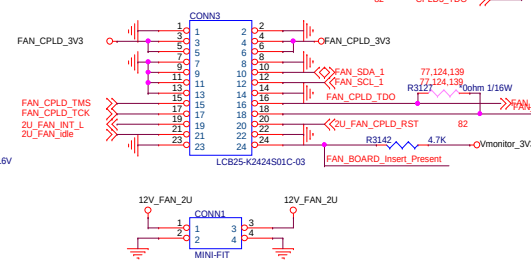
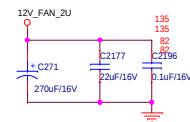
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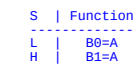
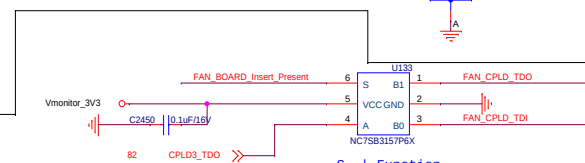
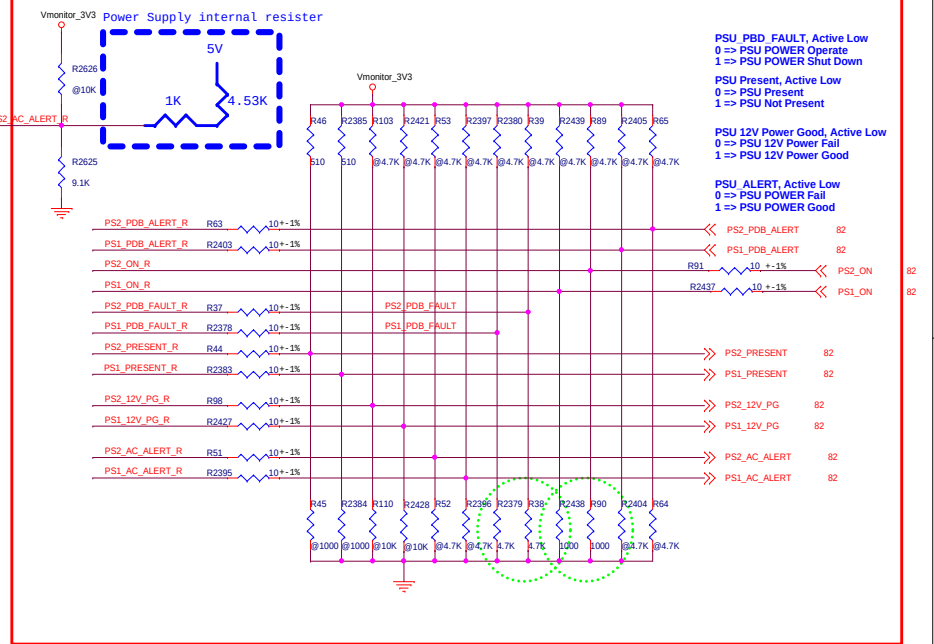
1U Fan Board CONN



2U Fan Board CONN



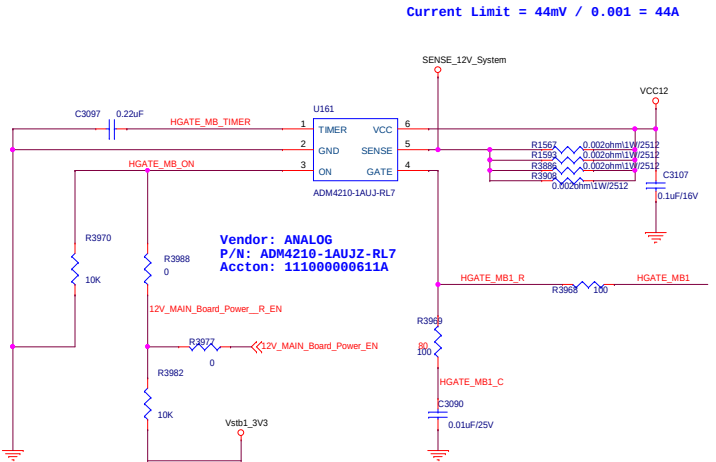
Power Module CONN



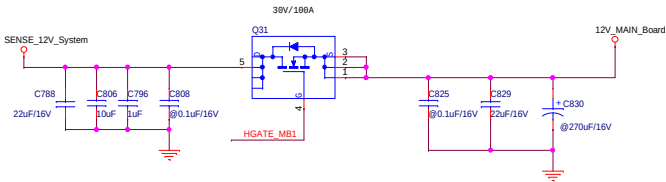
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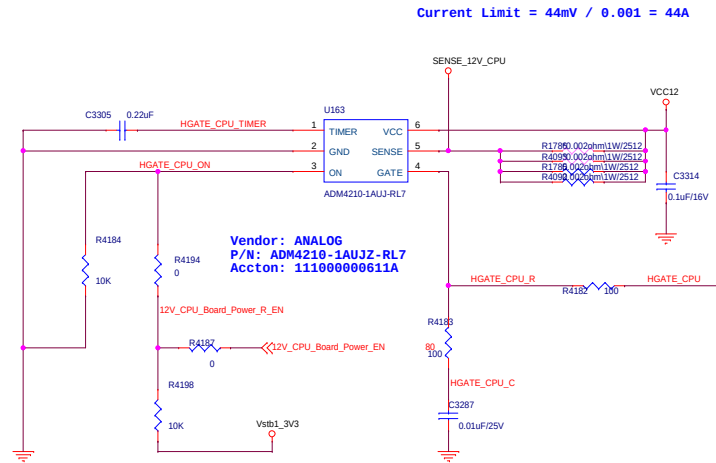
PSU to 12V(Main)



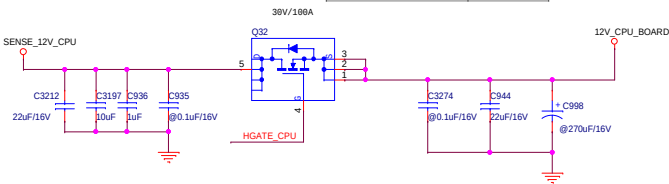
Product Summary:

BV _{DSS}	30V
R _{DS(ON)} (MAX.)	2.5mΩ
I _D	100A

115200000421A : Second source
Need change to Main source: 115200000360A



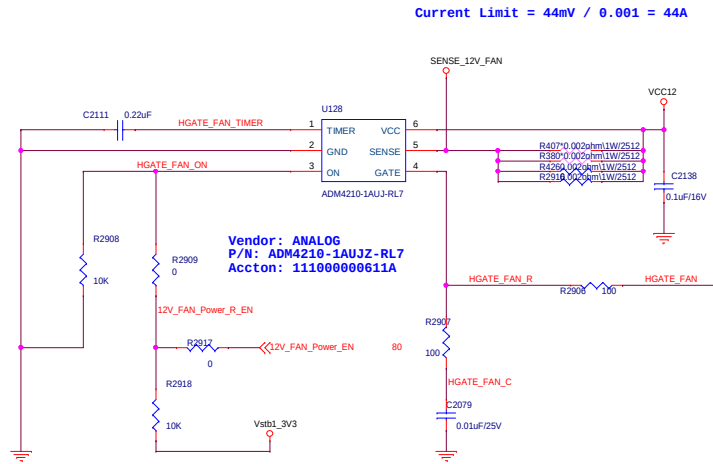
PSU to CPU board



Product Summary:

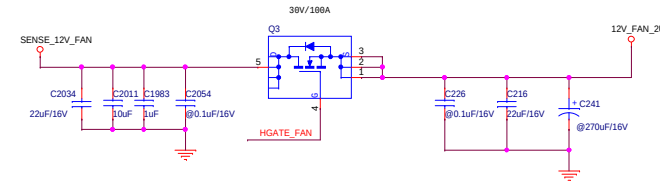
BV _{DSS}	30V
R _{DS(ON)} (MAX.)	2.5mΩ
I _D	100A

115200000421A : Second source
Need change to Main source: 115200000360A

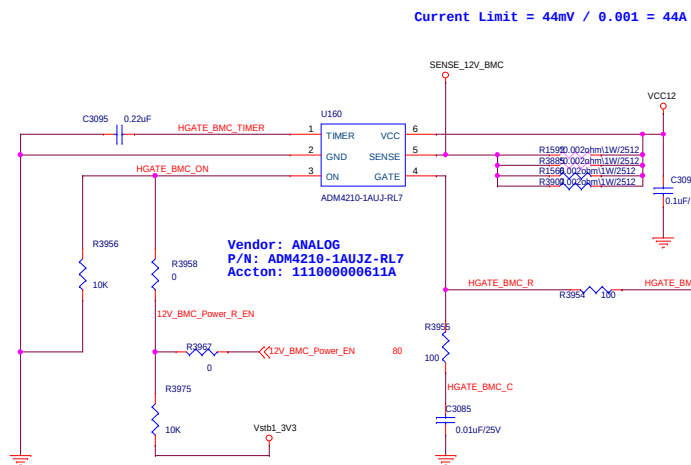


PSU to FAN board

Product Summary:	
BV _{DSS}	30V
R _{DS(on)} (MAX.)	2.5mΩ
I _D	100A

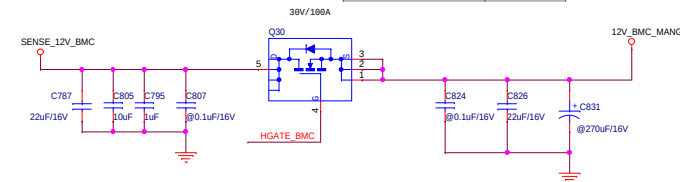


115200000421A : Second source
Need change to Main source: 115200000360A

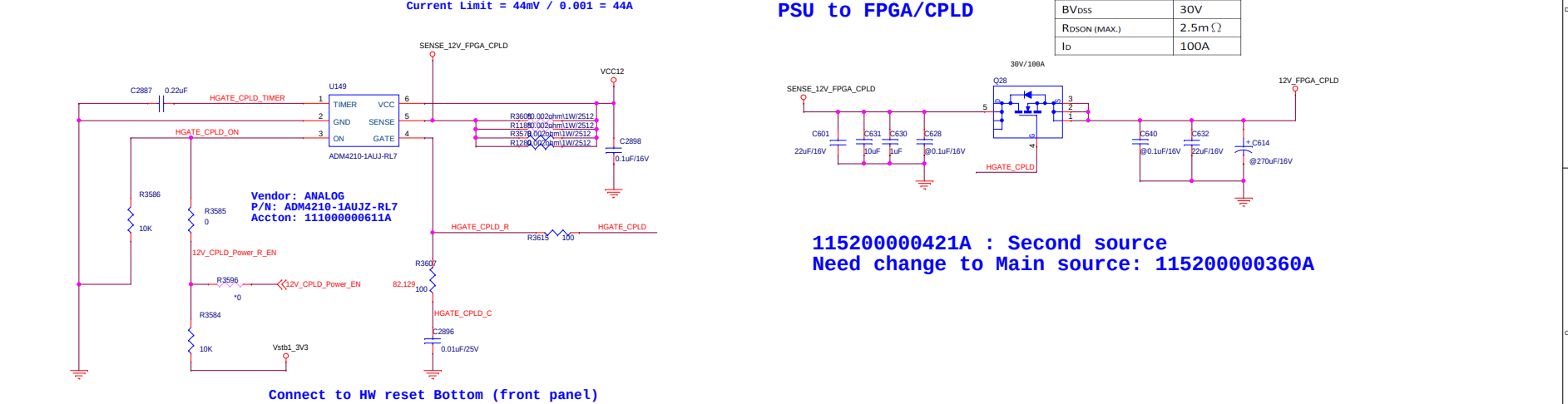


PSU to BMC board/MANG

Product Summary:	
BV _{DSS}	30V
R _{DS(on)} (MAX.)	2.5mΩ
I _D	100A

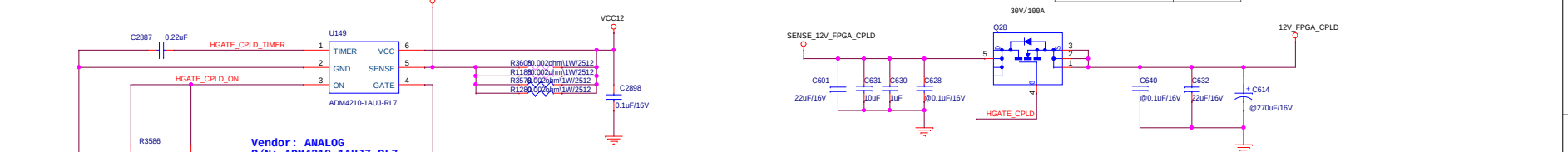


115200000421A : Second source
Need change to Main source: 115200000360A



$$\text{Current Limit} = 44\text{mV} / 0.001 = 44\text{A}$$

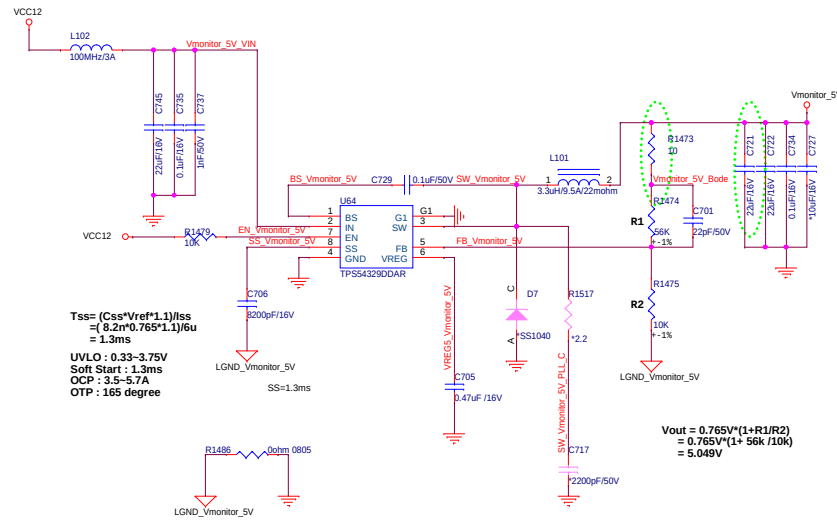
Current Limit = 44mV / 0.001 = 44A		PSU to FPGA/CPLD	
SENSE_12V_FPGA_CPLD		BV _{DSS}	30V
		R _{DS(on)} (MAX.)	2.5mΩ
		I _D	100A



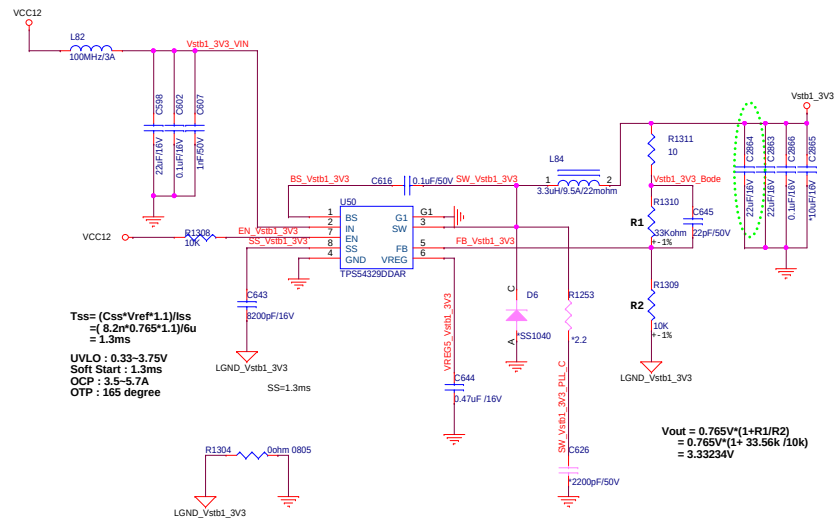
115200000421A : Second source
Need change to Main source: 115200000360A

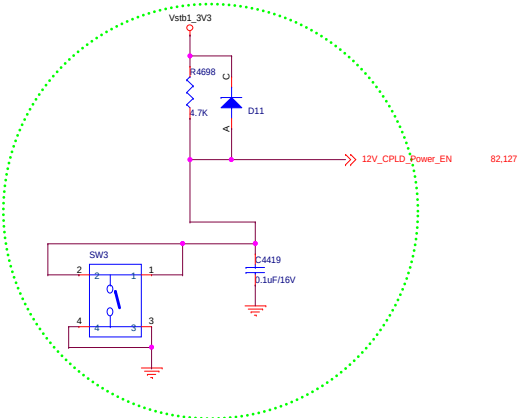
FMA-HW01008-01 R01

Vmonitor_5V / 1A



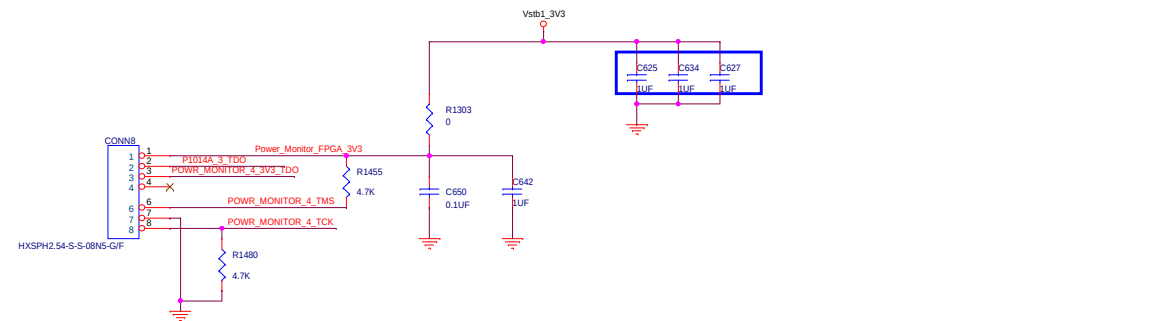
Vstb1_3V3 / 1A



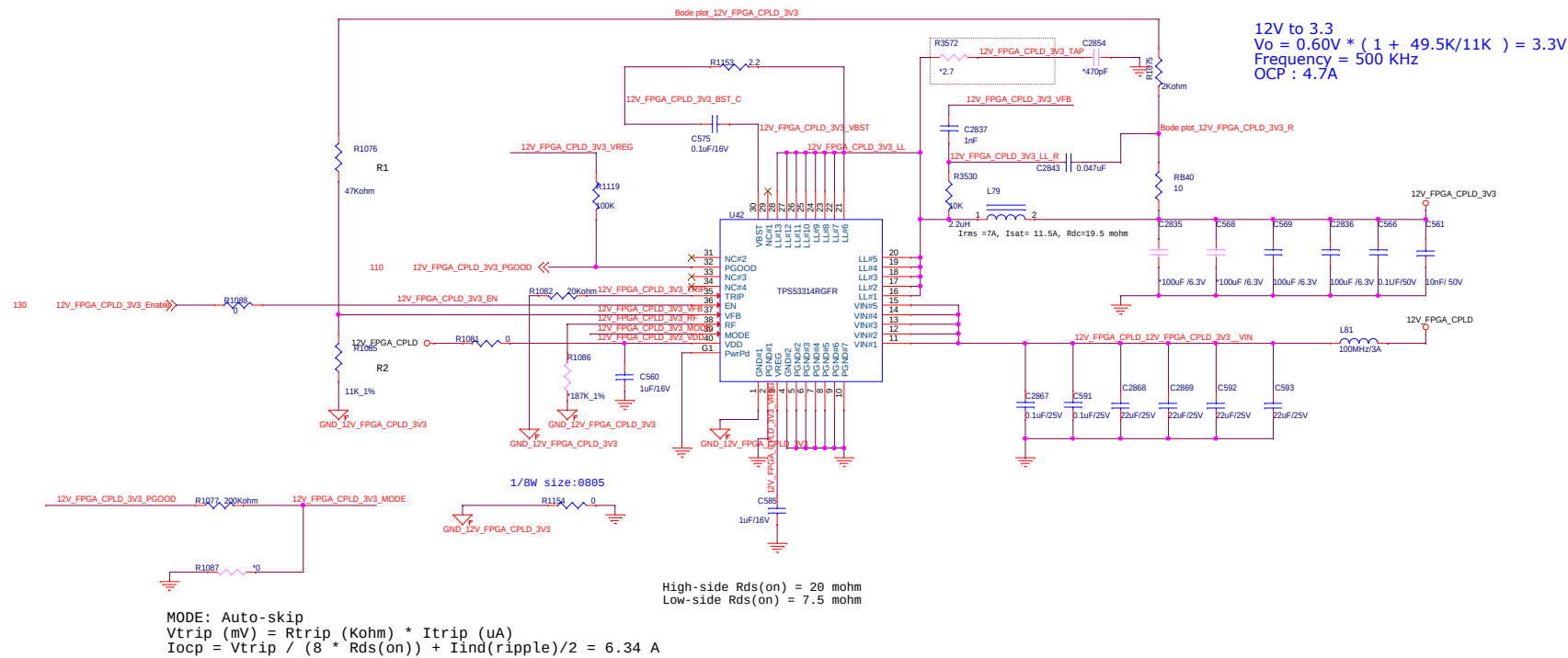


For Front port Reset Button(ZZ)

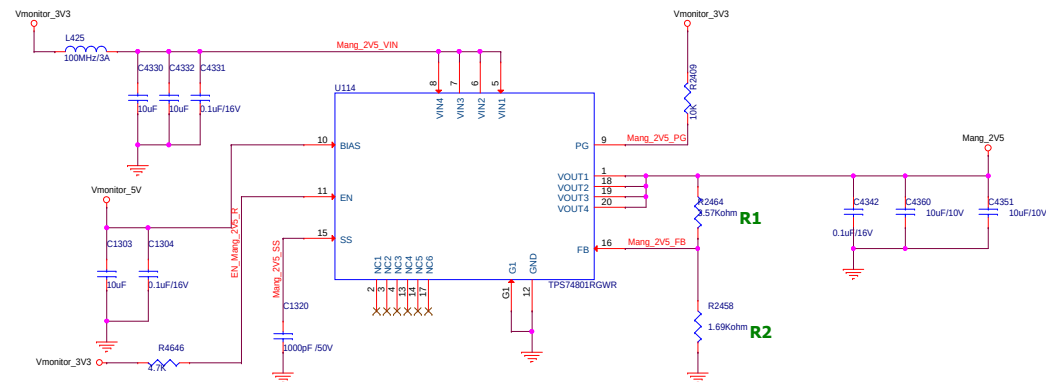
NEED check VMON1 can as OUT4 reference



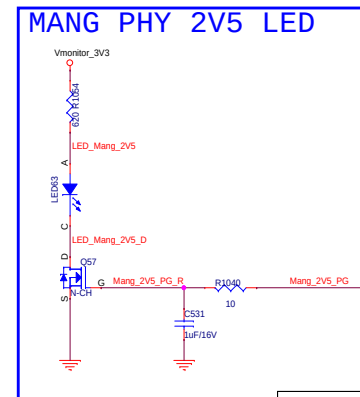
Mang_2V5/ 0.421A



```
MODE: Auto-skip
Vtrip (mV) = Rtrip (Kohm) * Itrip (uA)
Iocp = Vtrip / (8 * Rds(on)) + Iind(ripple)/2 = 6.34 A
```

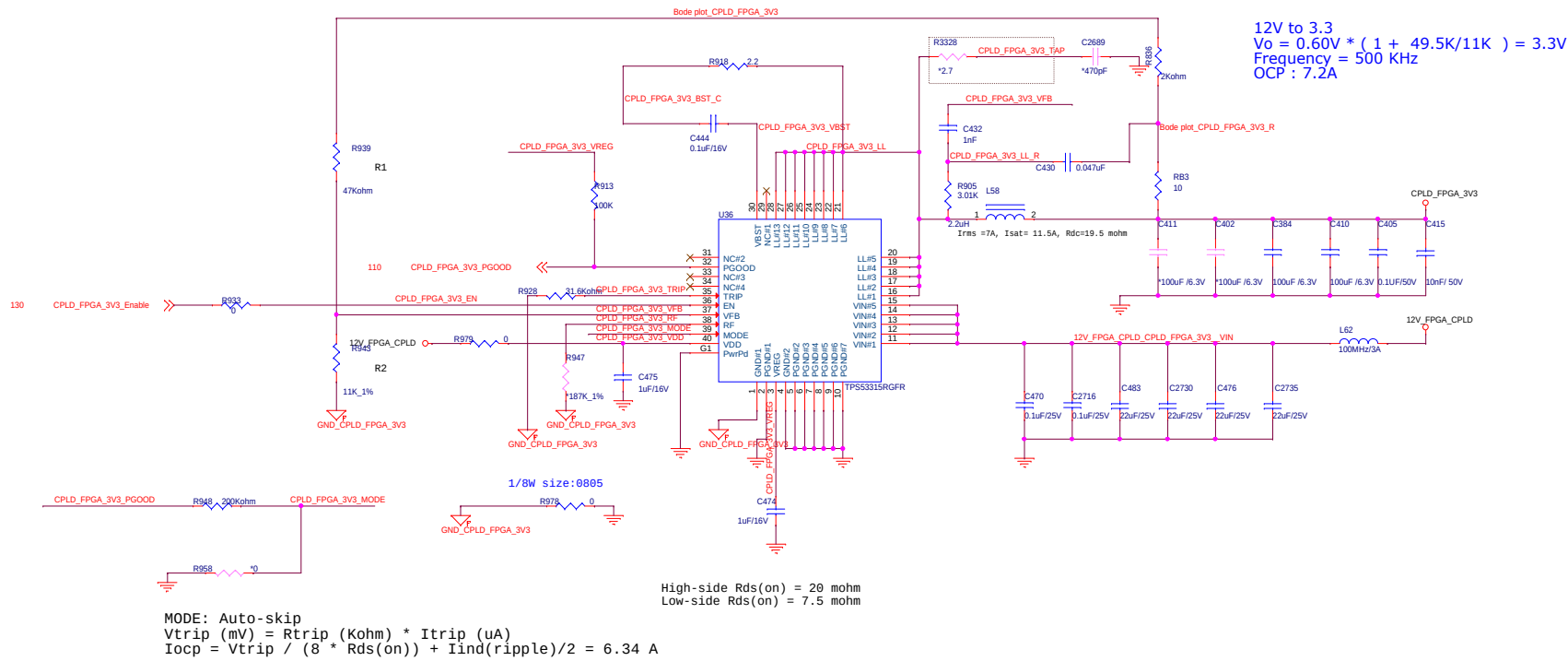


MAX Current=1.5A(TPS74801)

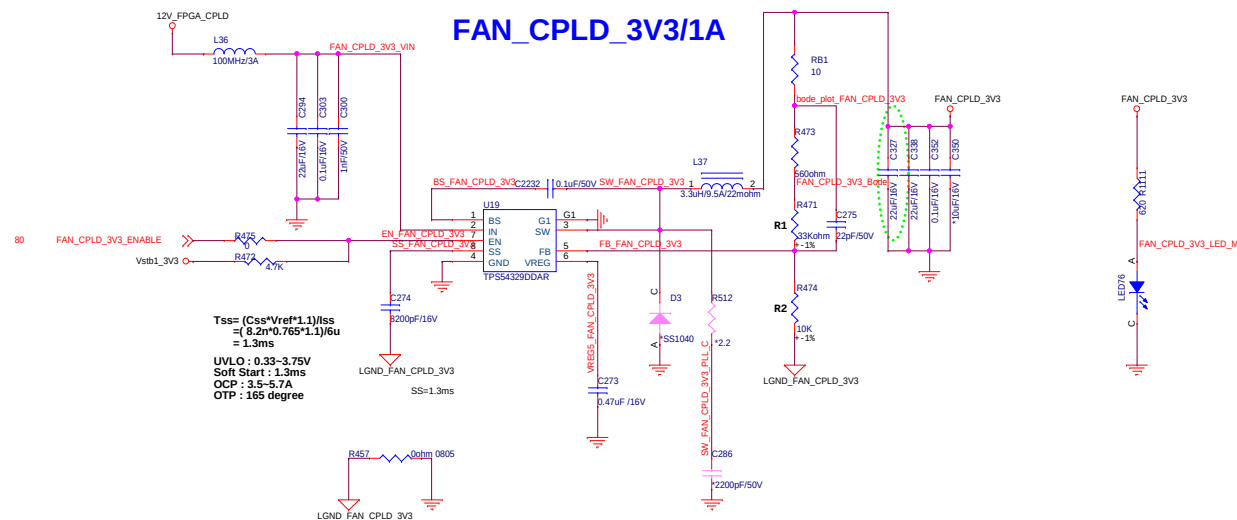


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CPLD_FPGA_3V3/5A

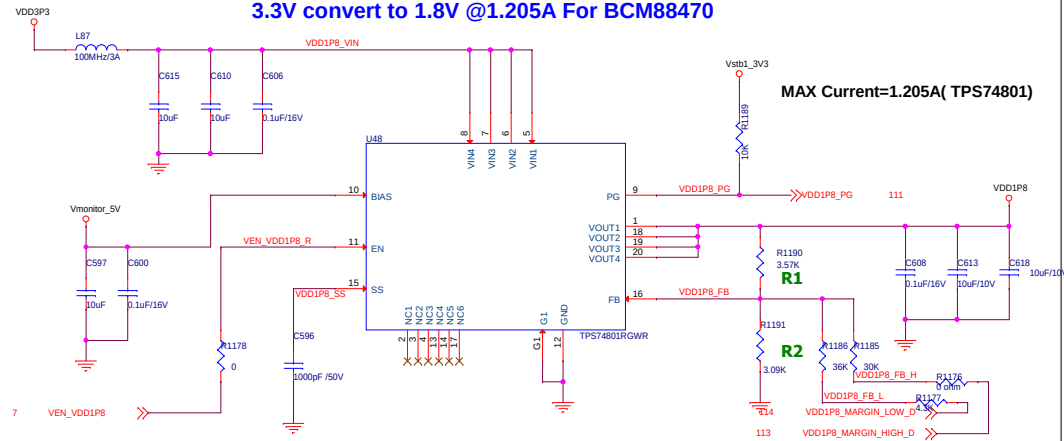


FAN_CPLD_3V3/1A



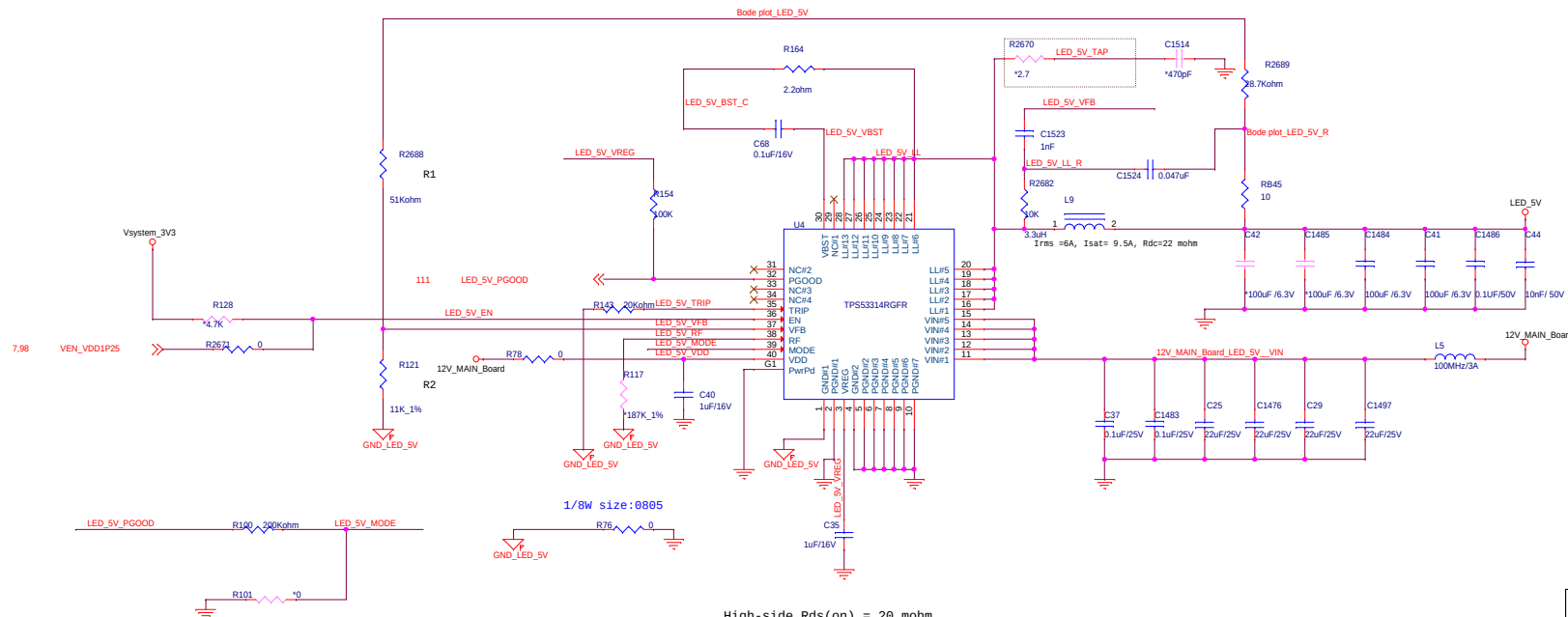
3.3V convert to 1.8V @1.205A For BCM88470

MAX Current=1.205A(TPS74801)



LED_5V/ 3A

12V to 5V
 $V_o = 0.60V * (1 + 81K/11K) = 5.01V$
 Frequency = 500 KHz
 OCP : 4.5A



MODE: Auto-skip
 $V_{trip} (mV) = R_{trip} (Kohm) * I_{trip} (uA)$
 $I_{ocp} = V_{trip} / (8 * R_{ds(on)}) + I_{ind(ripple)}/2 = 6.34 A$

High-side Rds(on) = 20 mohm
 Low-side Rds(on) = 7.5 mohm



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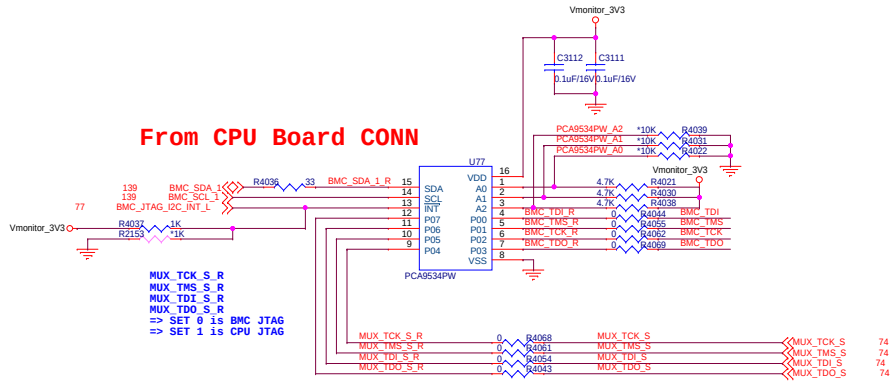
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For Power Monitor, CPLD

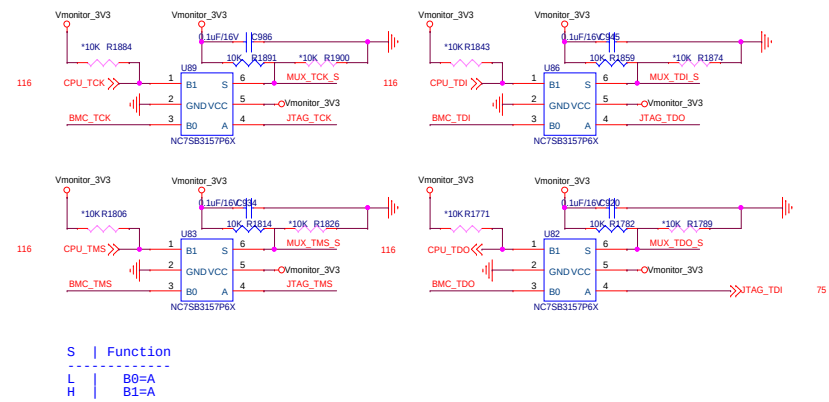


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C		<Doc>			
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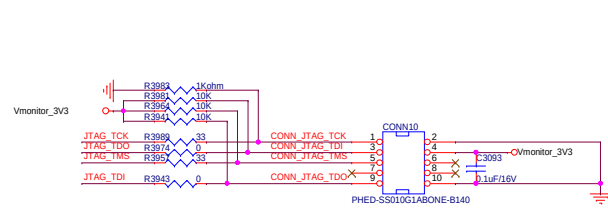
BMC JTAG I/O EXP



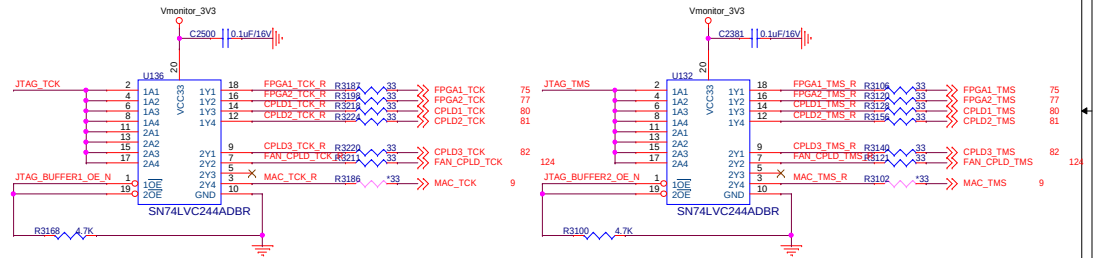
CPU/BMC JTAG MUX



JTAG CONN

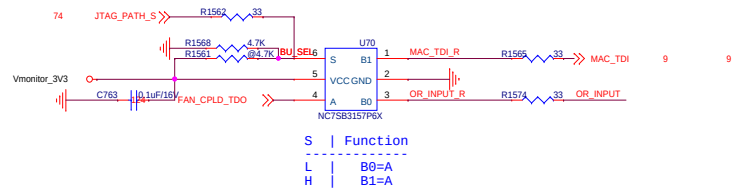


TCK/TMS BUFFER

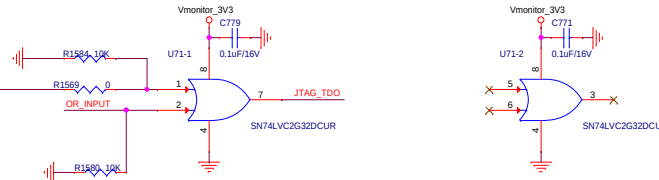


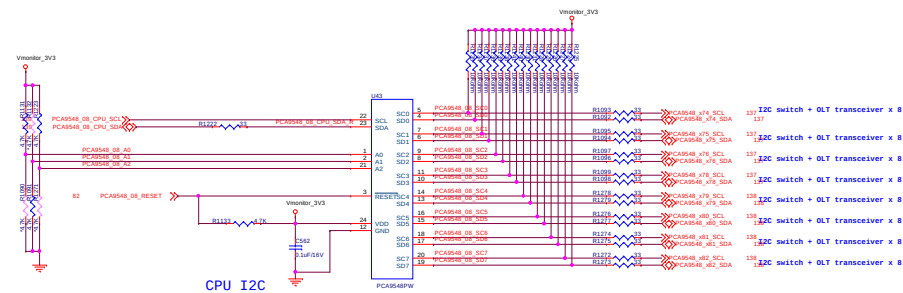
JTAG MUX TO PHY/OR

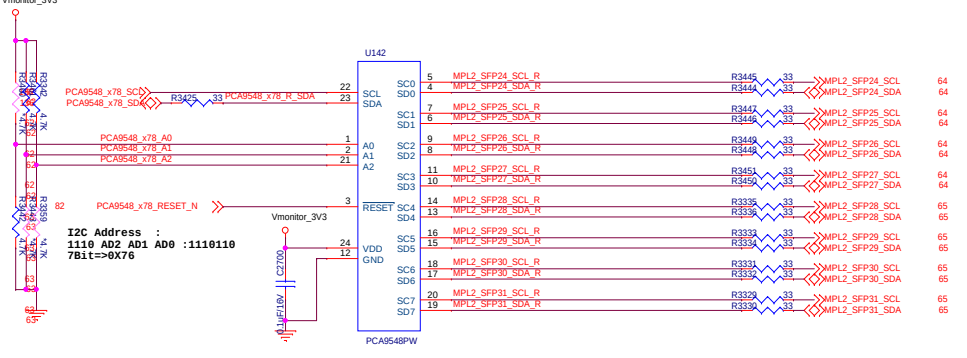
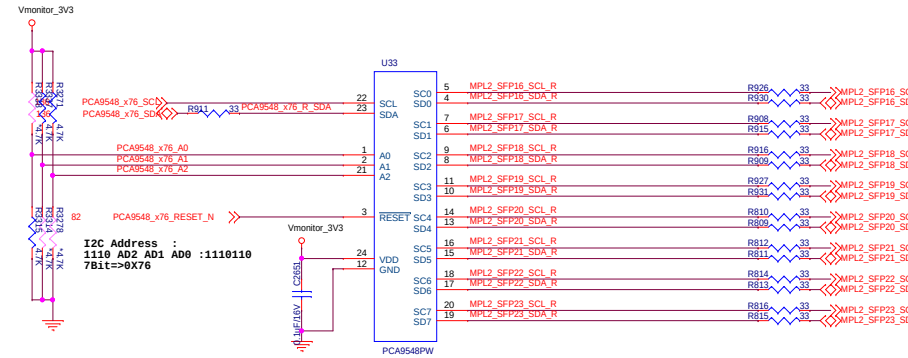
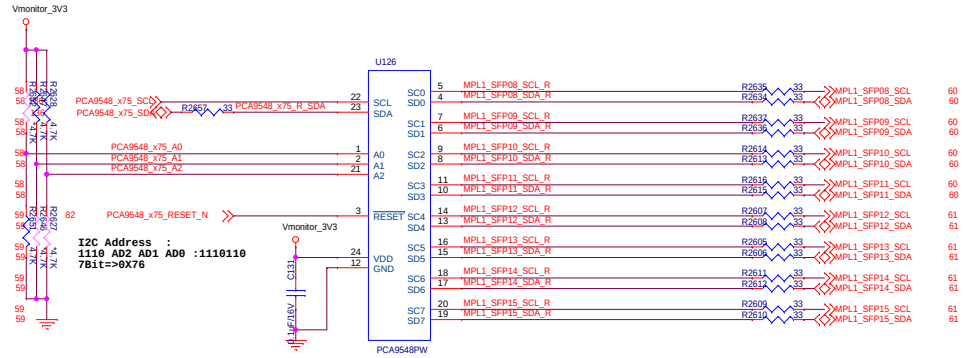
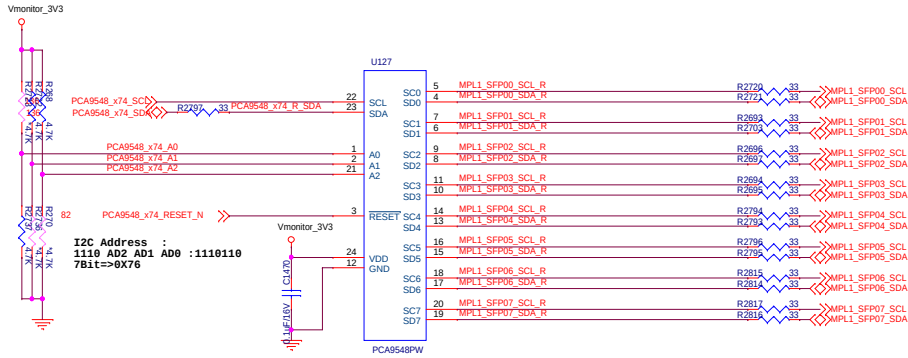
0 : Not Select 88470 JATG Path
Default Set to 0 : when 0 cannot update CPLD/FPGA code

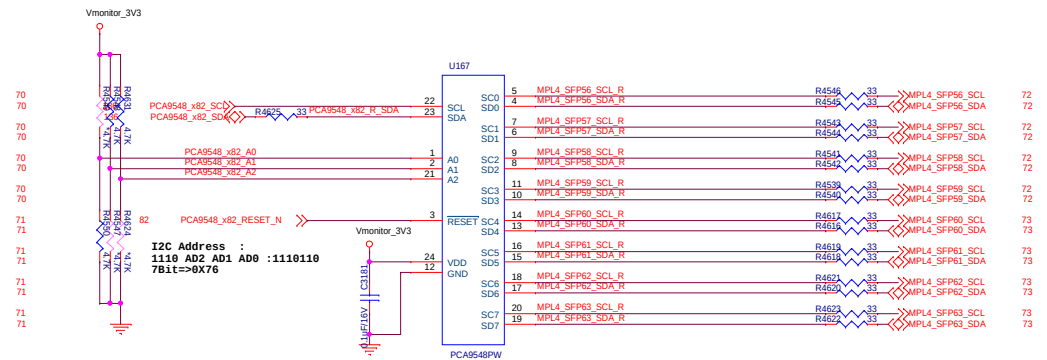
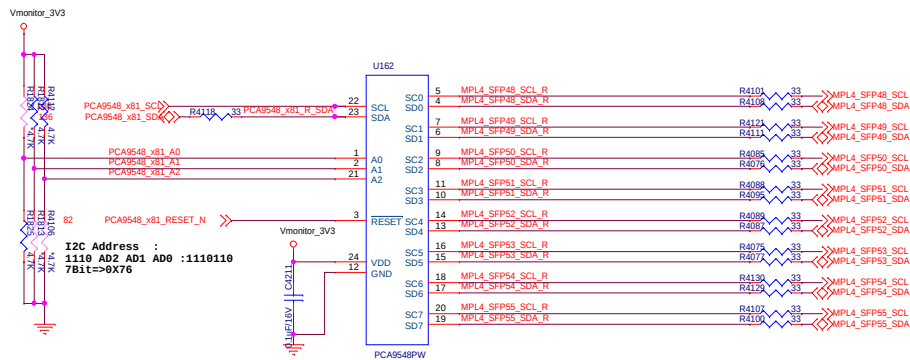
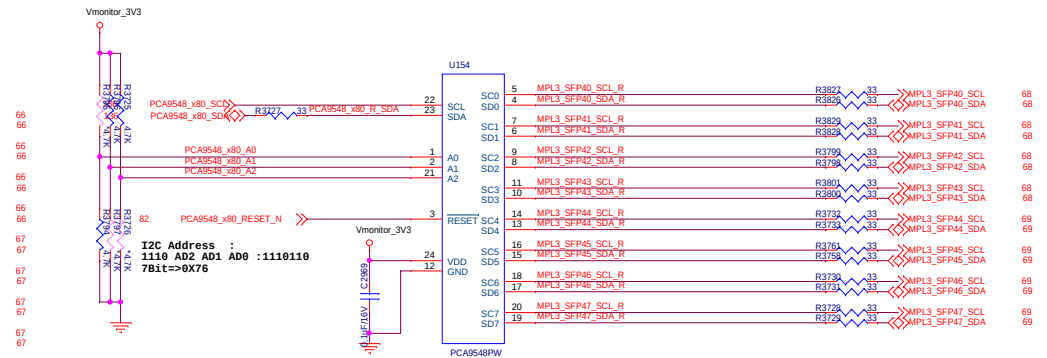
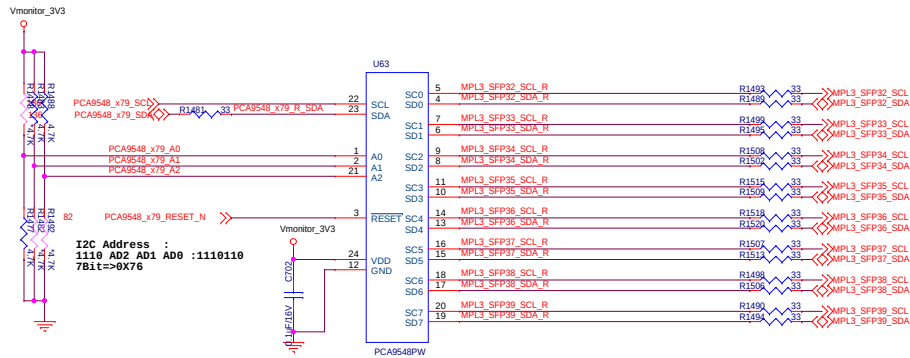


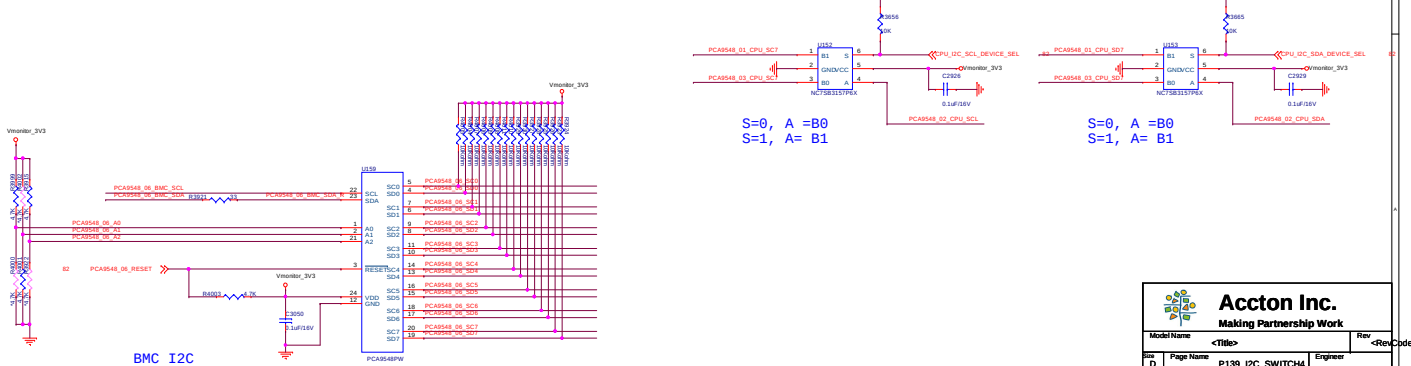
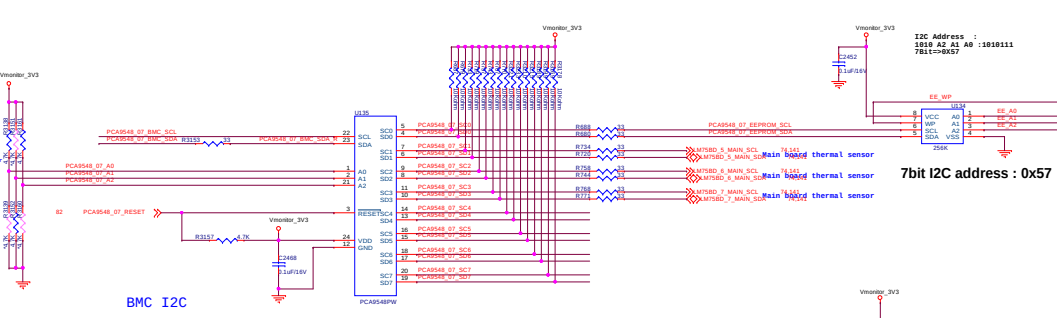
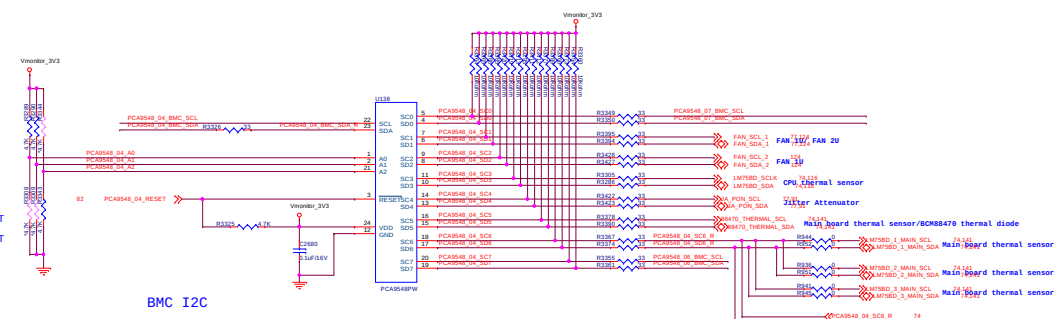
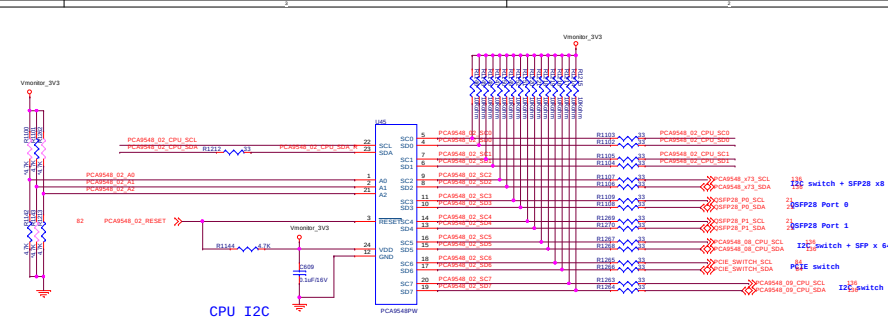
OR GATE TO JTAG TDO

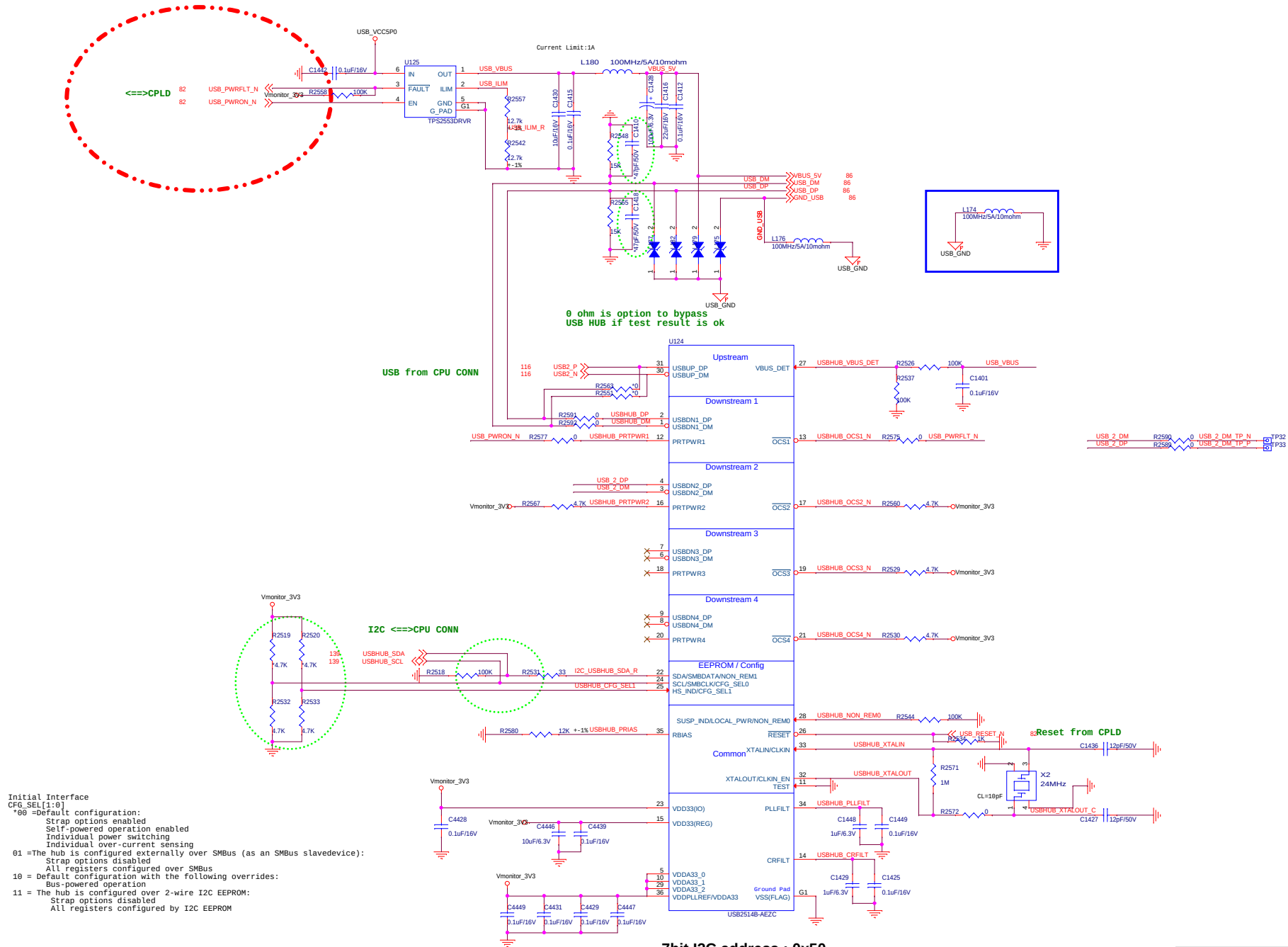


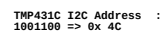












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